06-24-02 A10:30 IN

4231 69439

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

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Date 6/21/02 Serial # 09/993,967 Priority Application Date 6/12/00

Your Name M. Lewis Examiner # _____

AU 2823 Phone 305-3743 Room Plaza 3-3807

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-8

Problem: See Page 5 lines 1-21

Solution: " " " 23-29
" 6 " 1-17
+ Abstract

Novelty is in the structure

Staff Use Only

Searcher: Anne Hendrickson

Searcher Phone: 605-1726

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 6/25/02

Date Completed: 6/27/02

Searcher Prep/Rev Time: 60 min

Online Time: 180 min

Type of Search

Structure (#) _____
Bibliographic X
Litigation _____
Fulltext X
Patent Family _____
Other _____

Vendors

STN X
Dialog X
Questel/Orbit _____
Lexis-Nexis _____
WWW/Internet _____
Other _____

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?ds

Set      Items   Description
S1       11520   DRAM OR DYNAMIC()RANDOM()ACCESS()(MEMORY OR MEMORIES)
S2           0   MC=(U11-C18A3 OR U13-D07)
S3       11520   S1 OR S2
S4      239696   TRENCH? OR GROOVE? OR TRACK?
S5        3987   S4 AND S3
S6       23332   STRAP?
S7         224   S5 AND S6
S8         172   S7 AND TRANSISTOR?
S9         153   S8 AND CAPACITOR?
S10        122   S9 AND VERTICAL?
S11         26   S10 AND PERPENDICULAR?
S12        106   S8 AND DIFFUSION?
S13         72   S12 AND SIDEWALL?
S14         15   S11 AND SIDEWALL?
?show files
File 348:EUROPEAN PATENTS 1978-2002/Jun W03
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20020620,UT=20020613
         (c) 2002 WIPO/Univentio
?
```

.14/TI,PN,PD,AN,AD,AE/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Trench - capacitor vertical transistor DRAM **cell**
DRAM **Speicherzelle mit Grabenkondensator und vertikalem** Transistor
Cellule de memoire DRAM **avec un condensateur en tranchee et un** transistor vertical
PATENT (CC, No, Kind, Date): EP 1213761 A1 020612 (Basic)
APPLICATION (CC, No, Date): EP 2001127355 011121;
PRIORITY (CC, No, Date): JP 2000371106 001206

ABSTRACT EP 1213761 A1

A semiconductor device has an element substrate (10) including a semiconductor layer (13) of a first conductivity type being formed over a semiconductor substrate with (11) a dielectric film (12) interposed therebetween. A **groove** (20) is formed in the element substrate with a depth extending from a top surface of the semiconductor layer into the dielectric film, the **groove** having a width-increased **groove** portion (25) in the dielectric film as to expose a bottom surface of the semiconductor layer (13). An impurity diffusion source (23) is buried in the width-increased **groove** portion to be contacted with the bottom surface. A **transistor** (Q) is formed to have a first diffusion layer (31) being formed through impurity diffusion from the impurity diffusion source (23) to the bottom surface of the semiconductor layer, a second diffusion layer (32) formed through impurity diffusion to the top surface of the semiconductor layer, and a gate electrode (33a) formed at a side face of the **groove** over the impurity diffusion source with a gate insulation film (30) between the side face and the gate electrode.

14/TI,PN,PD,AN,AD,AE/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Method of micromachining a multi-part cavity
Verfahren zur Mikrobearbeitung einer Korperholung mit mehrfachem Profil
Methode pour la microfabrication d'une cavite a profil complexe
PATENT (CC, No, Kind, Date): EP 1077475 A2 010221 (Basic)
APPLICATION (CC, No, Date): EP 117155 000810;
PRIORITY (CC, No, Date): US 372477 990811

ABSTRACT EP 1077475 A2

The present disclosure pertains to our discovery of a particularly efficient method for etching a multi-part cavity in a substrate. The method provides for first etching a shaped opening, depositing a protective layer over at least a portion of the inner surface of the shaped opening, and then etching a shaped cavity directly beneath and in continuous communication with the shaped opening. The protective layer protects the etch profile of the shaped opening during etching of the shaped cavity, so that the shaped opening and the shaped cavity can be etched to have different shapes, if desired. In particular embodiments of the method of the invention, lateral etch barrier layers and/or implanted etch stops are also used to direct the etching process. The method of the invention can be applied to any application where it is necessary or desirable to provide a shaped opening and an underlying shaped cavity having varying shapes. The method is also useful whenever it is necessary to maintain tight control over the dimensions of the shaped opening.

14/TI,PN,PD,AN,AD,AE/3 (Item 3 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

DRAM **memory array with four cells per bit line contact**
DRAM **-Speichermatrix mit vier Zellen pro Bitleitungskontakt**
Reseau de memoire DRAM **avec quatre cellules pour chaque contact de ligne de bit**
PATENT (CC, No, Kind, Date): EP 991124 A2 000405 (Basic)
APPLICATION (CC, No, Date): EP 99116439 990821;

PRIORITY (CC, No, Date): US 163670 980930

ABSTRACT EP 991124 A2

A cell-quadropole cell structure is disclosed which extends the principle of sharing the bitline-stud between two different cells (arranged in a one-dimensional line, e.g. w-direction) further to the maximal possible degree of a sharing in a two-dimensional area (x- and y-direction) consequently forming a cross of four cells around one bitline-stud with each drain region and buried **strap** extended to the side and the **trench** attached forming a hook like structure.

14/TI,PN,PD,AN,AD,AE/4 (Item 4 from file: 348)

Vertical transistor DRAM **cell and method of producing the same**
DRAM **-Zelle mit vertikalem** Transistor **und Verfahren zur Herstellung derselben**
Cellule DRAM **a** transistor vertical **et son procede de manufacture**

PATENT (CC, No, Kind, Date): EP 964448 A2 991215 (Basic)
APPLICATION (CC, No, Date): EP 99103997 990311;
PRIORITY (CC, No, Date): US 95793 980611

ABSTRACT EP 964448 A2

A semiconductor device includes a substrate forming a **trench** , the **trench** including a storage node disposed within the **trench** . A wordline is disposed within the substrate and adjacent to a portion of the substrate. A **vertically** disposed **transistor** is included wherein the wordline functions as a gate, the storage node and a bitline function as one of a source and a drain such that when activated by the wordline the **transistor** conducts between the storage node and the bitline. The invention further includes a method of fabricating the semiconductor device with **vertical transistors** .

14/TI,PN,PD,AN,AD,AE/5 (Item 5 from file: 348)

Vertical transistor **implemented in a memory cell comprising a** trench capacitor
Vertikaler Transistor **implementiert in einer Speicherzelle mit Grabenkondensator**
Transistor verticale **pour les cellules de memoires composees de capacite ensillonnee**

PATENT (CC, No, Kind, Date): EP 905783 A1 990331 (Basic)
APPLICATION (CC, No, Date): EP 98115567 980819;
PRIORITY (CC, No, Date): US 940649 970930

ABSTRACT EP 905783 A1

A **vertical transistor** (258) used in a memory cell, such as a **DRAM** cell, having a **trench capacitor** (210). The **vertical transistor** (258) comprises a gate which includes a horizontal portion (253) and a **vertical** portion (245) located above the **trench capacitor** (210).

14/TI,PN,PD,AN,AD,AE/6 (Item 6 from file: 348)

DRAM trench capacitor **with enlarged surface**
DRAM **Grabenkondensator mit vergrosserter Oberflache**
Capacite ensillonee de type DRAM **avec surface augmentee**

PATENT (CC, No, Kind, Date): EP 903782 A2 990324 (Basic)
EP 903782 A3 011010
APPLICATION (CC, No, Date): EP 98115818 980821;
PRIORITY (CC, No, Date): US 932926 970919

ABSTRACT EP 903782 A2

A **DRAM** cell utilizes to form its storage **capacitor** a **trench** whose lower portion formed in a n-type substrate is etched electrochemically to provide the walls of such portion with large pores (31A). The porous walls are coated with a dielectric (26B) and the **trench** then filled with doped polysilicon (24A). There results a **capacitor** with a very large surface area and a high capacitance.

14/TI,PN,PD,AN,AD,AE/7 (Item 7 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Trench capacitor dram **cell with** vertical transistor
DRAM **-Zelle mit Graben-Kondensator und vertikalem** Transistor
Cellule DRAM **a capacite ensillonee avec** transistor vertical
PATENT (CC, No, Kind, Date): EP 884785 A2 981216 (Basic)
EP 884785 A3 011010
APPLICATION (CC, No, Date): EP 98109684 980528;
PRIORITY (CC, No, Date): US 872780 970611

ABSTRACT EP 884785 A2
A **vertical transistor** used in a memory cell, such as a **DRAM** cell, having a **trench capacitor** . The **vertical transistor** comprises a gate which includes a horizontal portion and a **vertical** portion located above the **trench capacitor** .

14/TI,PN,PD,AN,AD,AE/8 (Item 8 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

High density trench capacitor DRAM **cell**
Grabenkondensator- DRAM **-Zelle hoher Dichte**
Cellule DRAM **a haute densite ayant un condensateur ensillone**
PATENT (CC, No, Kind, Date): EP 720221 A1 960703 (Basic)
APPLICATION (CC, No, Date): EP 95480175 951206;
PRIORITY (CC, No, Date): US 365617 941228

ABSTRACT EP 720221 A1
The present invention is a **DRAM** cell, comprising a **transistor** having a gate, the gate having an individual segment of gate conductor (17) and a conductive spacer rail wordline (66,67) in contact with the segment gate. The wordline connector is formed by directional etching a conductor formed along a **sidewall** above the gate segment. The **sidewall** is formed by etching a **groove** in a mandrel (60). The structure permits design of a five square folded-bitline **DRAM** cell. (see image in original document) (see image in original document)

14/TI,PN,PD,AN,AD,AE/9 (Item 9 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Three-dimensional semiconductor structures formed from planar layers.
Dreidimensionale Halbleiterstrukturen geformt aus ebenen Schichten.
Structures tridimensionnelles a semi-conducteur formees par des couches planares.
PATENT (CC, No, Kind, Date): EP 424623 A2 910502 (Basic)
EP 424623 A3 910724
EP 424623 B1 950712
APPLICATION (CC, No, Date): EP 90115752 900817;
PRIORITY (CC, No, Date): US 427679 891026

ABSTRACT EP 424623 A2
Three-dimensional semiconductor structures are taught in which various device types are formed from a plurality of planar layers (16, 18) on a substrate (10). The major process steps include the formation of a plurality of alternating layers of material (16, 18), including semiconductor and dielectric materials, forming a **vertical** access hole (19) in the layers, processing the layers selectively to form active or

passive semiconductor devices, and filling the access hole (19) with a conductor. The ultimate structure includes a three-dimensional memory array in which entire dynamic memory cells are fabricated in a stacked **vertical** orientation above support circuitry formed on a planar surface.

14/TI,PN,PD,AN,AD,AE/10 (Item 10 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Fabrication process for a self-aligned, lightly-doped drain-source trench transistor .
Verfahren zur Herstellung eines sichselbstjustierenden Transistors **mit schwach dotiertem Drain und Source in einem Graben.**
Methode de fabrication d'un transistor **auto-aligne avec source et drain legerement dope formes dans une tranchee.**
PATENT (CC, No, Kind, Date): EP 399191 A1 901128 (Basic)
EP 399191 B1 940824
APPLICATION (CC, No, Date): EP 90106685 900406;
PRIORITY (CC, No, Date): US 355232 890522

ABSTRACT EP 399191 A1
A structure and fabrication process for a self-aligned, lightly-doped drain/source n-channel field-effect **transistor** wherein a **trench** is formed in a well region (15) in a wafer including an epitaxial layer (12) on a substrate (10). A first, heavily doped drain region and bit line element (18) is formed around the **trench** on the surface of the well (15) , and a second, lightly-doped drain region (24) is formed proximate to the first drain region (18) and self-aligned to the **trench sidewalls** . A source region (26) is located beneath the **trench** , which is filled with polysilicon (32), above which is gate and further polysilicon forming a transfer wordline (33). The gate polysilicon (32) is separated from the **trench** side walls by a layer (30) of gate oxide insulation. The well region (15) at the **trench sidewalls** are doped to control the device threshold level, and the device is thereby also located at a wordline/bitline cross-point.

14/TI,PN,PD,AN,AD,AE/11 (Item 11 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

HIGH-PERFORMANCE DRAM **ARRAYS INCLUDING** TRENCH CAPACITORS .
DRAM **-ARRAYS HOHER LEISTUNG MIT GRABEN-KONDENSATOREN.**
RESEAUX DE MEMOIRES VIVES DYNAMIQUES DE HAUTE PERFORMANCE COMPRENANT DES CONDENSATEURS A TRANCHEES.
PATENT (CC, No, Kind, Date): EP 232361 A1 870819 (Basic)
EP 232361 B1 920930
WO 8700690 870129
APPLICATION (CC, No, Date): EP 86905002 860708; WO 86US1426 860708
PRIORITY (CC, No, Date): US 758885 850725

14/TI,PN,PD,AN,AD,AE/12 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

METHOD FOR HYBRID DRAM **CELL UTILIZING CONFINED** STRAP **ISOLATION**
PROCEDE DESTINE A UNE CELLULE DRAM **HYBRIDE METTANT EN OEUVRE UNE ISOLATION DE CONNEXION ENFOUIE**
Patent and Priority Information (Country, Number, Date):
Patent: WO 200237542 A2 20020510 (WO 0237542)
Application: WO 2001US46921 20011105 (PCT/WO US0146921)

English Abstract
A process of forming a hybrid memory cell which is scalable to a minimum feature size, F, of about 60 nm at an operating voltage of V"sub"blh of about 1.5 V and substantially free of floating-well effects.

14/TI,PN,PD,AN,AD,AE/13 (Item 2 from file: 349)

AN INTEGRATED CIRCUIT COMPRISING A SELF ALIGNED TRENCH **, AND METHOD OF FORMING THEREOF**
CIRCUIT INTEGRE A TRANCHEE AUTO-ALIGNEE ET SON PROCEDE DE REALISATION
Patent and Priority Information (Country, Number, Date):
Patent: WO 200229889 A2 20020411 (WO 0229889)
Application: WO 2001US29194 20010919 (PCT/WO US0129194)

English Abstract
An integrated circuit comprising a **vertically** oriented device formed with a substantially SELF ALIGNED process, in which the **trench** , active area (e.g., 128, 228), and gate (e.g., 132, 232) of a **DRAM** cell may be formed using a minimal number of masks and lithographic steps. Using this process, a **DRAM** cell comprising a **vertical transistor** and a buried word line (e.g., 132, 232) may be formed. A gate dielectric (e.g., 130, 230) may be disposed adjacent the active area, and the portion of the buried word line adjacent the gate dielectric may function as the **vertically** oriented gate for the **vertical transistor** . The **DRAM** memory cell may comprise one of a variety of **capacitors** , such a **trench capacitor** underlying the **vertical transistor** , or a stack **capacitor** (e.g., 241) overlying the **vertical transistor** . When a stack **capacitor** is used, a buried bit line (e.g., 208) underlying the **vertical transistor** may also be used.

14/TI,PN,PD,AN,AD,AE/14 (Item 3 from file: 349)

SELF ALIGNED TRENCH **AND METHOD OF FORMING THE SAME**
TRANCHEE AUTO-ALIGNEE ET PROCEDE DE FORMATION DE CETTE DERNIERE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200225730 A2 20020328 (WO 0225730)
Application: WO 2001US42263 20010924 (PCT/WO US0142263)

English Abstract
A method of forming a **trench** can be used in the fabrication of **dynamic random access memory** (**DRAM**) cells. In one aspect, a first layer of a first material (e.g., polysilicon) is formed over a semiconductor region (e.g., a silicon substrate). The first layer is patterned to remove portions of the first material. A second material (e.g., oxide) can then be deposited to fill the portions where the first material was removed. After removing the remaining portions of the first layer of first material, a **trench** can be etched in the semiconductor region. The **trench** would be substantially aligned to the second material.

14/TI,PN,PD,AN,AD,AE/15 (Item 4 from file: 349)

HIGH-PERFORMANCE DRAM **ARRAYS INCLUDING** TRENCH CAPACITORS
RESEAUX DE MEMOIRES VIVES DYNAMIQUES DE HAUTE PERFORMANCE COMPRENANT DES CONDENSATEURS A TRANCHEES
Patent and Priority Information (Country, Number, Date):
Patent: WO 8700690 A1 19870129
Application: WO 86US1426 19860708 (PCT/WO US8601426)

English Abstract
Parallel elongated **trenches** (22) in a silicon substrate (11, 12) are utilized to form multiple distinct memory cell **capacitors** on each continuous wall (24, 26) of each **trench** . Chanstops (52) are formed between adjacent **capacitors** to achieve electrical isolation. A separate word line (64) overlies each **trench** wall and is connected via respective MOS **transistors** to the spaced-apart **capacitors** formed on the wall. A reliable high-density memory characterized by excellent

performance is thereby realized.

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?ds

Set      Items   Description
S1       18191   DRAM OR DYNAMIC()RANDOM()ACCESS()(MEMORY OR MEMORIES)
S2           0   MC=(U11-C18A3 OR U13-D07)
S3       18191   S1 OR S2
S4      522874   TRENCH? OR GROOVE? OR TRACK?
S5        1222   S4 AND S3
S6       10201   STRAP?
S7          47   S5 AND S6
S8          18   S7 AND TRANSISTOR?
S9          16   S8 AND CAPACITOR?
S10          7   S9 AND VERTICAL?
S11          0   S10 AND PERPENDICULAR?
S12          2   S8 AND DIFFUSION?
S13          0   S12 AND SIDEWALL?
S14     104152   CC=(B1265D OR B2570 OR B2550)
S15     117669   S1 OR S14
S16       3331   S15 AND S4
S17         49   S16 AND S6
S18         18   S17 AND TRANSISTOR?
S19          8   S18 AND VERTICAL?
S20          5   RD (unique items)
S21        505   S16 AND TRANSISTOR?
S22         50   S21 AND VERTICAL?
S23          1   S22 AND PERPENDICULAR?
S24         26   S22 AND CAPACITOR?
S25          0   S24 AND DIFFUSION?
S26          7   S24 AND SIDEWALL?
?show files
File   2:INSPEC 1969-2002/Jun W4
         (c) 2002 Institution of Electrical Engineers
File   6:NTIS 1964-2002/Jul W1
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
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         (c) 2002 Engineering Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2002/Jun W5
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
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         (c) 2002 ProQuest Info&Learning
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         (c) 2002 BLDSC all rts. reserv.
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         (c) 2002 Cambridge Sci Abs
File  94:JICST-EPlus 1985-2002/May W1
         (c)2002 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2002/May
         (c) 2002 The HW Wilson Co.
File 108:Aerospace Database 1962-2002/Jun
         (c) 2002 AIAA
File 144:Pascal 1973-2002/Jun W4
         (c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Jun
         (c) 2002 Reed-Elsevier (UK) Ltd.
File 305:Analytical Abstracts 1980-2002/Jun W3
         (c) 2002 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2001/Dec
         (c) 2002 DECHEMA
?
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?t s23/9/1

23/9/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04412486 JICST ACCESSION NUMBER: 00A0066770 FILE SEGMENT: JICST-E
IEDM 99.
KAWANE TOSHIAKI (1)
Gekkan Semiconductor World(Semiconductor World), 1999, VOL.18,NO.12, PAGE.74-75, FIG.2
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: IEDM'99 (Washington D.C. on 12/5-12/9th, 1999)was held. This is a report from the meeting. This time, there was a proposal of the epoch-making **transistor** structure in CMOS device in which the limit for the refinement began to be seen from the viewpoint of power consumption and lithography. It is a **transistor** (VRG MOSFET) of the **vertical** structure in which gate,source and drain are fabricated **perpendicularly** to the substrate. Lucent Technology reported a **transistor** of the 50nm gate length and Infineon/IBM reported a **vertical transistor** (VERI VEST) for the **DRAM trench** cell.
DESCRIPTORS: **transistor** ; longitudinal type; gate circuit; MOSFET; chemical vapor deposition; **DRAM**
IDENTIFIERS: Lucent Technology; Infineon Technologies; IBM; IEDM99
BROADER DESCRIPTORS: semiconductor device; solid state device; type; circuit; MISFET; FET; vapor deposition; RAM; memory(computer); equipment; dynamic memory
CLASSIFICATION CODE(S): NC03070N
?

?t s26/9/3,4,7

26/9/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03157394 INSPEC Abstract Number: B88039725
Title: A practical trench isolation technology with a novel planarization
Author(s): Fuse, G.; Ogawa, H.; Tateiwa, K.; Kakao, I.; Odanaka, S.; Fukumoto, M.; Iwasaki, H.; Ohzone, T.
Author Affiliation: Matsushita Electr. Ind. Co. Ltd., Osaka, Japan
Conference Title: 1987 International Electron Devices Meeting, IEDM. Technical Digeset (Cat. No.87CH2515-5) p.732-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1987 Country of Publication: USA 936 pp.
U.S. Copyright Clearance Center Code: CH2515-5/87/0000-0732$01.00
Conference Sponsor: IEEE
Conference Date: 6-9 Dec. 1987 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The **vertical - trench** isolation method utilizes a thin SiO/sub 2/ film between double photoresists for uniform top-resist coating and for an etch-back barrier, a poly-silicon film above active regions for an etch-back buffer and large tilt-angle boron ion implantations into the **trench - sidewalls** for narrow-channel-effect control. The planarization with the resist/oxide/resist and the poly silicon (PRORPS) can isolate the whole surface of a 6-in-diameter wafer very uniformly with a large process margin. The standard deviation of the threshold voltage of an n-channel MOSFET (W/L=10 mu m/0.8 mu m) over the whole wafer is 0.38% at about 0.5-V threshold voltage. The narrow-channel-effect is controlled for FETs down to 0.5- mu m channel width. The method is applied to the megabit SCC (surrounded **capacitor** cell) dynamic RAM and the cells and the peripheral circuits are isolated at the same time. (9 Refs)
Subfile: B
Descriptors: field effect integrated circuits; insulated gate field effect **transistors** ; integrated circuit technology; ion implantation; photoresists; semiconductor technology; VLSI
Identifiers: polysilicon film; threshold voltage standard deviation; surrounded **capacitor** cell **DRAM** ; **trench** isolation technology; planarization; double photoresists; uniform top-resist coating; etch-back barrier; ion implantations; **trench - sidewalls** ; narrow-channel-effect control; PRORPS; n-channel MOSFET; narrow-channel-effect; channel width; 0.5 V; 0.5 micron; thin SiO/sub 2/ film; Si:B
Class Codes: **B2550** (Semiconductor device technology); B2550G (Lithography); B2560R (Insulated gate field effect transistors); B2570F (Other MOS integrated circuits
Chemical Indexing:
SiO2 int - O2 int - Si int - O int - SiO2 bin - O2 bin - Si bin - O bin (Elements - 2)
Si:B int - Si int - B int - Si:B bin - Si bin - B bin - Si el - B el - B dop (Elements - 1,1,2)
Numerical Indexing: voltage 5.0E-01 V; size 5.0E-07 m

26/9/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

02867733 INSPEC Abstract Number: B87024190
Title: Characterization of trench transistors of 3-D memories
Author(s): Banerjee, S.K.; Shichijo, H.; Nishimura, A.; Shah, A.H.; Pollack, G.P.; Richardson, W.F.; Bordelon, M.; Malhi, S.D.S.; Elahy, M.; Womack, R.H.; Wang, C.P.; Gallia, J.; Davis, H.E.; Chatterjee, P.K.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Conference Title: 1986 Symposium on VLSI Technology. Digest of Technical

Papers p.79-80
Publisher: Japan Soc. Appl. Phys, Tokyo, Japan
Publication Date: 1986 Country of Publication: Japan 90 pp.
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 28-30 May 1986 Conference Location: San Diego, CA, USA
Availability: IEEE, Piscataway, NJ, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: An innovative, 9- mu m/sup 2/ **DRAM** cell with both the pass **transistor** and the storage **capacitor** on the **sidewalls** of a **trench** has been demonstrated in a 4-Mb **DRAM** and previously reported. The characteristics of the **vertical trench transistor** , which is the key new element in the structure, are discussed. It is shown that pass **transistors** can be reproducibly fabricated on the **sidewalls** of a **trench** , and that these devices are well behaved. They have adequate threshold voltage and subthreshold slope, and low leakage to allow cell functionality in a 4-Mb **DRAM** . (3 Refs)
Subfile: B
Descriptors: field effect integrated circuits; integrated memory circuits ; random-access storage
Identifiers: **trench** sidewalk; **trench transistors** ; **DRAM** cell; pass **transistor** ; storage **capacitor** ; **vertical trench transistor** ; threshold voltage; subthreshold slope; low leakage; 4 Mbit
Class Codes: **B1265D** (Memory circuits); B2570H (Other field effect integrated circuits
Numerical Indexing: storage capacity 4.2E+06 bit

26/9/7 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02239225 E.I. Monthly No: EIM8704-022608
Title: CHARACTERIZATION OF TRENCH TRANSISTORS **FOR 3-D MEMORIES.**
Author: Banerjee, S. K.; Shichijo, H.; Nishimura, A.; Shah, A. H.; Pollack, G. P.; Richardson, W. F.; Bordelon, M.; Malhi, S. D. S.; Elahy, M. ; Womack, R. H.; Wang, C. P.; Gallia, J.; Davis, H. E.; Chatterjee, P. K.
Corporate Source: Texas Instruments Inc, Dallas, TX, USA
Conference Title: 1986 Symposium on VLSI Technology - Digest of Technical Papers.
Conference Location: San Diego, CA, USA Conference Date: 19860528
Sponsor: IEEE Electron Devices Soc, New York, NY, USA; Japan Soc of Applied Physics, Jpn
E.I. Conference No.: 09244
Source: Digest of Technical Papers - Symposium on VLSI Technology 1986. Publ by Business Cent for Academic Soc Japan, Tokyo, Jpn. Available from IEEE Service Cent (Cat n 86CH2318-4), Piscataway, NJ, USA p 79-80
Publication Year: 1986
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8704
Abstract: An innovative, 9- MU m**2 **DRAM** cell with both the pass **transistor** and the storage **capacitor** on the **sidewalls** of a **trench** has been demonstrated in a 4-Mb **DRAM** and previously reported. The characteristics of the **vertical trench transistor** , which is the key new element in the structure, are discussed. It is shown that pass **transistors** can be reproducibly fabricated on the **sidewalls** of a **trench** , and that these devices are well behaved. They have adequate threshold voltage and subthreshold slope, and low leakage to allow cell functionality in a 4-Mb **DRAM** . 3 refs.
Descriptors: DATA STORAGE, SEMICONDUCTOR; **TRANSISTORS** ; DATA STORAGE, DIGITAL--Random Access
Identifiers: **TRENCH CAPACITORS** ; 3-D MEMORIES; 4-MB **DRAM** ; PASS **TRANSISTORS**
Classification Codes:

6/9/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

7015018 INSPEC Abstract Number: B2001-10-1265D-002, C2001-10-7410D-007
Title: 2.4F/sup 2/ memory cell technology with stacked-surrounding gate transistor **(S-SGT)** DRAM
Author(s): Endoh, T.; Suzuki, M.; Sakuraba, H.; Masuoka, F.
Author Affiliation: Res. Inst. of Electr. Commun., Tohoku Univ., Sendai, Japan
Journal: IEEE Transactions on Electron Devices Conference Title: IEEE Trans. Electron Devices (USA) vol.48, no.8 p.1599-603
Publisher: IEEE,
Publication Date: Aug. 2001 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
SICI: 0018-9383(200108)48:8L.1599:MCTW;1-4
Material Identity Number: I037-2001-008
U.S. Copyright Clearance Center Code: 0018-9383/2001/$10.00
Conference Title: ESSDERC 2000. 30th European Solid-State Device Research Conference
Conference Date: 11-13 Sept. 2000 Conference Location: Cork, Ireland
Document Number: S0018-9383(01)05752-5
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: This paper proposes 2.4F/sup 2/ memory cell technology with stacked-surrounding gate **transistor** (S-SGT) **DRAM** . One unit of the S-SGT **DRAM** is formed by stacking several SGT-type cells in series **vertically** . The SGT-type cell itself arranges gate, source, drain and plate on a silicon pillar **vertically** . Both gate and plate electrode surround the silicon pillar. Subsequently applied **trench** etching and sidewall spacer formation during S-SGT **DRAM** formation causes a step-like silicon pillar structure. Due to these steps, gate, plate and diffusion layer in one S-SGT **DRAM** unit are fabricated **vertically** by a self-aligned process. The cell size dependence of the self-aligned-type S-SGT **DRAM** was analyzed with regard to the above step widths and the number of cells in one unit. As a result, the cell design for minimizing the cell size of this device has been formulated. By using the proposed cell design, it is demonstrated by process simulation that the S-SGT **DRAM** in 0.5 mu m design rule can achieve a cell size of 2.4F/sup 2/, which is half of the cell size of a conventional SGT **DRAM** cell (4.8F/sup 2/). Therefore, the S-SGT **DRAM** is a promising candidate for future ultra high density DRAMs. (8 Refs)
Subfile: B C
Descriptors: cellular arrays; **DRAM** chips; etching; integrated circuit design; memory architecture; semiconductor process modelling
Identifiers: 2.4F/sup 2/ memory cell technology; stacked-surrounding gate **transistor** **DRAM** ; SGT-type cells; **trench** etching; sidewall spacer formation; diffusion layer; self-aligned process; cell size dependence; process simulation; design rule; ultra high density DRAMs; 0.5 micron
Class Codes: B1265D (Memory circuits); B2550X (Semiconductor process modelling and simulation); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); B1265A (Digital circuit design, modelling and testing); B2550E (Surface treatment (semiconductor technology)); C7410D (Electronic engineering computing)
Numerical Indexing: size 5.0E-07 m

6/9/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC
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03811205 INSPEC Abstract Number: B91008287, C91009992
Title: A new 0.5 mu m/sup 2/ DRAM **cell with internal charge gain investigated by 2D transient device simulation**
Author(s): Richter, R.; Ehwald, K.E.; Heinemann, B.; Matzke, W.-E.; Gajewski, H.; Winkler, W.

Author Affiliation: Inst. for Phys. of Semicond., Acad. of Sci., Frankfurt Oder, East Germany
Conference Title: ESSDERC 90. 20th European Solid State Device Research Conference p.177-80
Editor(s): Eccleston, W.; Rosser, P.J.
Publisher: Adam Hilger, Bristol, UK
Publication Date: 1990 Country of Publication: UK xxix+637 pp.
ISBN: 0 7503 0065 5
Conference Sponsor: IEE; IEEE; EPS
Conference Date: 10-13 Sept. 1990 Conference Location: Nottingham, UK
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P)
Abstract: The **Vertically** Integrated Gain (VIG) cell is a new **DRAM** structure for 64/256 Mbit DRAMs. By using a **trench** structure and 0.25 mu m design rules a cell size of 0.55 mu m/sup 2/ is attainable. The cell function bases on merging 2 bipolar junction **transistors** (BJT), 1 junction field effect **transistor** (JFET) and 2 capacitors. 2D transient device simulation is used to investigate the electrical behaviour of the VIG cell. A high read out signal, 2 control lines, operation voltages between 0 and 5 volts only and the capability to maintain the stored information during read operation are the main features of the proposed **DRAM** cell. (3 Refs)
Subfile: B C
Descriptors: digital simulation; **DRAM** chips; VLSI
Identifiers: VIG cell; **DRAM** cell; internal charge gain; 2D transient device simulation; **Vertically** Integrated Gain; **trench** structure; design rules; bipolar junction **transistors** ; junction field effect **transistor** ; electrical behaviour; read out signal; control lines; operation voltages; read operation; 64 to 256 Mbit; 0.25 micron
Class Codes: B1265D (Memory circuits); C5320G (Semiconductor storage); C7410D (Electronic engineering)
Numerical Indexing: storage capacity 6.7E+07 to 2.68E+08 bit; size 2.5E-07 m

6/9/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

03669169 INSPEC Abstract Number: B90043152, C90046294
Title: A composed trench transistor **(CTT) cell for 16/64 MB dRAMs**
Author(s): Richardson, W.F.; Anderson, D.N.; Shen, B.W.; Solowiej, E.J.; Chen, I.C.; Teng, I.C.; McAdams, H.P.; Holland, W.B.; Redwine, D.J.; Stiegler, H.J.; Herndon, T.H.; Price, C.; Nasu, T.; Loh, W.K.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Conference Title: 1989 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.89CH2694-8) p.65-6
Publisher: Business Center for Acad. Soc. Japan, Tokyo, Japan
Publication Date: 1989 Country of Publication: Japan xiii+107 pp.
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 22-25 May 1989 Conference Location: Kyoto, Japan
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A CTT cell has been developed for and incorporated into a 16-MB **dRAM** . Due to the area advantage derived from **vertical** integration, the 16-MB **dRAM** chip operates at 5 V with no internal regulation and fits in a 400-mil SOI package. The cell structure allows **transistor** and diffusion isolation sizes to be large enough to support full 5 V operation. Since cell characteristics are determined by **trench** profiles and **vertical** lithography, it is potentially scalable to the 64 MB generation. (4 Refs)
Subfile: B C
Descriptors: CMOS integrated circuits; integrated memory circuits; random-access storage
Identifiers: **DRAM** ; dynamic RAM; twin tube CMOS process; composed **trench transistor** ; CTT cell; **vertical** integration; SOI package; diffusion isolation; 16 Mbit; 64 Mbit; 5 V
Class Codes: B1265D (Memory circuits); B2570D (CMOS integrated circuits);

C5320G (Semiconductor storage)
Numerical Indexing: storage capacity 1.7E+07 bit; storage capacity 6.7E+07 bit; voltage 5.0E+00 V

6/9/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

03621949 INSPEC Abstract Number: B90027322, C90034278
Title: A study on a new high density DRAM **cell**
Author(s): Cheon Hee Yi
Author Affiliation: Dept. of Electr. Eng., Chongju Univ., Seoul, South Korea
Journal: Journal of the Korean Institute of Telematics and Electronics vol.26, no.6 p.124-30
Publication Date: June 1989 Country of Publication: South Korea
Language: Korean Document Type: Journal Paper (JP)
Treatment: New Developments (N); Practical (P)
Abstract: Innovations in fabrication process and circuit design which have led to dramatic density improvement are discussed from the designer's perspective. A new **Trench** Epitaxial **Transistor** Cell has been developed for use in future megabit DRAMs. The storage electrode with n+-polysilicon and n+-source electrode are self-contacted. With the storage capacitance large enough to prevent soft errors, the cell size is reduced to 30% compared with existing BSE cells by use of the **vertical** capacitor made along the isolation region. (10 Refs)
Subfile: B C
Descriptors: integrated memory circuits; MOS integrated circuits; random-access storage
Identifiers: **trench** epitaxial **transistor** cell; storage electrode; high density **DRAM** cell; fabrication process; circuit design; source electrode; storage capacitance; cell size; **vertical** capacitor; isolation region
Class Codes: B1265D (Memory circuits); B2570F (Other MOS integrated circuits); C5320G (Semiconductor storage)

6/9/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

03398657 INSPEC Abstract Number: B89042166
Title: A buried- trench DRAM **cell using a self-aligned epitaxy over** trench **technology**
Author(s): Lu, N.C.C.; Rajeevakumar, T.V.; Bronner, G.B.; Ginsberg, B.; Machesney, B.J.; Sprogis, E.J.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: International Electron Devices Meeting. Technical Digest (IEEE Cat. No.88CH2528-8) p.588-91
Publisher: IEEE, New York, NY, USA
Publication Date: 1988 Country of Publication: USA 902 pp.
U.S. Copyright Clearance Center Code: CH2528-8/88/0000-0588$01.00
Conference Sponsor: IEEE
Conference Date: 11-14 Dec. 1988 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P); Experimental (X)
Abstract: A novel three-dimensional buried **trench** (BT) memory cell, suitable for **DRAM** (dynamic random access memories) of 64 Mb or beyond, has been demonstrated. It uses a novel self-aligned-epitaxy-over- **trench** (SEOT) technology which allows the fabrication of the cell horizontal access **transistor** in bulk material epitaxially grown over the **trench** capacitor. The via connection between the access **transistor** and the buried **trench** is a **vertical** sublithographic contact self-aligned to the **trench** . This BT cell, with a minimum of 10.8 lithographic squares, was

fabricated in a submicron n-well epitaxial CMOS process incorporating the SEOT technology. (4 Refs)
Subfile: B
Descriptors: CMOS integrated circuits; integrated circuit technology; integrated memory circuits; random-access storage; semiconductor epitaxial layers; VLSI
Identifiers: 3D buried **trench** memory cell; ULSI; buried- **trench** **DRAM** cell; dynamic random access memories; self-aligned-epitaxy-over- **trench** ; SEOT; **trench** capacitor; via connection; **vertical** sublithographic contact self-aligned; submicron n-well epitaxial CMOS process; 64 Mbit
Class Codes: B1265D (Memory circuits); B2570D (CMOS integrated circuits); B0510D (Epitaxial growth)
Numerical Indexing: storage capacity 6.7E+07 bit

6/9/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

03366926 INSPEC Abstract Number: B89029449, C89032722
Title: Advanced cell structures for dynamic RAMs
Author(s): Lu, N.C.C.
Author Affiliation: IMB Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: IEEE Circuits and Devices Magazine vol.5, no.1 p.27-36
Publication Date: Jan. 1989 Country of Publication: USA
CODEN: ICDMEN ISSN: 8755-3996
U.S. Copyright Clearance Center Code: 8755-3996/89/0100-0027$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Recent major progress in the area of advanced **DRAM** cell structures is described, focusing on three-dimensional approaches. Cell design criteria are first outlined. Then a number of structures are discussed, namely, the stacked-capacitor cell, the **trench** -capacitor cell, the substrate-plate **trench** -capacitor cell, the dielectrically insulated **trench** cell, the buried stacked-capacitor cell, the folded-capacitor cell, the isolation-merged **vertical** -capacitor cell, the buried-capacitor or stacked **transistor** cell, and the **trench** **transistor** cell. Future trends in cell structures are projected. (52 Refs)
Subfile: B C
Descriptors: cellular arrays; integrated memory circuits; random-access storage
Identifiers: cell design; advanced **DRAM** cell structures; three-dimensional approaches; stacked-capacitor cell; **trench** -capacitor cell; substrate-plate **trench** -capacitor cell; dielectrically insulated **trench** cell; buried stacked-capacitor cell; folded-capacitor cell; isolation-merged **vertical** -capacitor cell; buried-capacitor; stacked **transistor** cell; **trench** **transistor** cell
Class Codes: B1265D (Memory circuits); B2570 (Semiconductor integrated circuits); C5320G (Semiconductor storage)

6/9/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

03313810 INSPEC Abstract Number: B89016052
Title: The third dimension in microelectronics
Author(s): Gotzlich, J.
Journal: Physikalische Blaetter vol.44, no.10 p.391-5
Publication Date: Oct. 1988 Country of Publication: West Germany
CODEN: PHBLAG ISSN: 0031-9279
Language: German Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The author examines the use of depth as a means of increasing packing density in semiconducting devices yet further beyond that presently attained in 2-dimensions. (The present maximum is a 4-Mbit **DRAM** with

structures smaller than 1 micron). He describes in detail the two methods of utilising depth: i.e. **trench** techniques and 3D circuits. In particular he describes a **trench** capacitor and **vertical transistor** , explaining how each is made and the advantages and disadvantages, and then discusses silicon-on-insulator methods and their advantages and problems. He illustrates his descriptions with many detailed sections through semiconductor devices. (8 Refs)
Subfile: B
Descriptors: monolithic integrated circuits; semiconductor devices; semiconductor-insulator-semiconductor structures
Identifiers: microelectronics; depth; packing density; semiconducting devices; **DRAM** ; **trench** techniques; 3D circuits; **trench** capacitor; **vertical transistor** ; silicon-on-insulator methods; 4 Mbit; Si
Class Codes: B2570 (Semiconductor integrated circuits); B2530N (Other interfaces and junctions)
Chemical Indexing:
Si int - Si el (Elements - 1)
Numerical Indexing: storage capacity 4.2E+06 bit

6/9/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

03157394 INSPEC Abstract Number: B88039725
Title: A practical trench **isolation technology with a novel planarization**
Author(s): Fuse, G.; Ogawa, H.; Tateiwa, K.; Kakao, I.; Odanaka, S.; Fukumoto, M.; Iwasaki, H.; Ohzone, T.
Author Affiliation: Matsushita Electr. Ind. Co. Ltd., Osaka, Japan
Conference Title: 1987 International Electron Devices Meeting, IEDM. Technical Digeset (Cat. No.87CH2515-5) p.732-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1987 Country of Publication: USA 936 pp.
U.S. Copyright Clearance Center Code: CH2515-5/87/0000-0732$01.00
Conference Sponsor: IEEE
Conference Date: 6-9 Dec. 1987 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The **vertical - trench** isolation method utilizes a thin SiO/sub 2/ film between double photoresists for uniform top-resist coating and for an etch-back barrier, a poly-silicon film above active regions for an etch-back buffer and large tilt-angle boron ion implantations into the **trench** -sidewalls for narrow-channel-effect control. The planarization with the resist/oxide/resist and the poly silicon (PRORPS) can isolate the whole surface of a 6-in-diameter wafer very uniformly with a large process margin. The standard deviation of the threshold voltage of an n-channel MOSFET (W/L=10 mu m/0.8 mu m) over the whole wafer is 0.38% at about 0.5-V threshold voltage. The narrow-channel-effect is controlled for FETs down to 0.5- mu m channel width. The method is applied to the megabit SCC (surrounded capacitor cell) dynamic RAM and the cells and the peripheral circuits are isolated at the same time. (9 Refs)
Subfile: B
Descriptors: field effect integrated circuits; insulated gate field effect **transistors** ; integrated circuit technology; ion implantation; photoresists; semiconductor technology; VLSI
Identifiers: polysilicon film; threshold voltage standard deviation; surrounded capacitor cell **DRAM** ; **trench** isolation technology; planarization; double photoresists; uniform top-resist coating; etch-back barrier; ion implantations; **trench** -sidewalls; narrow-channel-effect control; PRORPS; n-channel MOSFET; narrow-channel-effect; channel width; 0.5 V; 0.5 micron; thin SiO/sub 2/ film; Si:B
Class Codes: B2550 (Semiconductor device technology); B2550G (Lithography); B2560R (Insulated gate field effect transistors); B2570F (Other MOS integrated circuits)
Chemical Indexing:

SiO2 int - O2 int - Si int - O int - SiO2 bin - O2 bin - Si bin - O bin (Elements - 2)
Si:B int - Si int - B int - Si:B bin - Si bin - B bin - Si el - B el - B dop (Elements - 1,1,2)
Numerical Indexing: voltage 5.0E-01 V; size 5.0E-07 m

6/9/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

02867733 INSPEC Abstract Number: B87024190
Title: Characterization of trench transistors **of 3-D memories**
Author(s): Banerjee, S.K.; Shichijo, H.; Nishimura, A.; Shah, A.H.; Pollack, G.P.; Richardson, W.F.; Bordelon, M.; Malhi, S.D.S.; Elahy, M.; Womack, R.H.; Wang, C.P.; Gallia, J.; Davis, H.E.; Chatterjee, P.K.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Conference Title: 1986 Symposium on VLSI Technology. Digest of Technical Papers p.79-80
Publisher: Japan Soc. Appl. Phys, Tokyo, Japan
Publication Date: 1986 Country of Publication: Japan 90 pp.
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 28-30 May 1986 Conference Location: San Diego, CA, USA
Availability: IEEE, Piscataway, NJ, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: An innovative, 9- mu m/sup 2/ **DRAM** cell with both the pass **transistor** and the storage capacitor on the sidewalls of a **trench** has been demonstrated in a 4-Mb **DRAM** and previously reported. The characteristics of the **vertical trench transistor** , which is the key new element in the structure, are discussed. It is shown that pass **transistors** can be reproducibly fabricated on the sidewalls of a **trench** , and that these devices are well behaved. They have adequate threshold voltage and subthreshold slope, and low leakage to allow cell functionality in a 4-Mb **DRAM** . (3 Refs)
Subfile: B
Descriptors: field effect integrated circuits; integrated memory circuits ; random-access storage
Identifiers: **trench** sidewalk; **trench transistors** ; **DRAM** cell; pass **transistor** ; storage capacitor; **vertical trench transistor** ; threshold voltage; subthreshold slope; low leakage; 4 Mbit
Class Codes: B1265D (Memory circuits); B2570H (Other field effect integrated circuits)
Numerical Indexing: storage capacity 4.2E+06 bit

6/9/18 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02863959 E.I. Monthly No: EIM9002-008376
Title: Novel test structure to study location of breakdown for trench **capacitor.**
Author: Kishi, K.; Yoshida, T.; Watanabe, T.; Tanaka, T.; Shinozaki, S.
Corporate Source: Toshiba Corp, Kawasaki, Jpn
Conference Title: Proceedings of the 1989 International Conference on Microelectronic Test Structures
Conference Location: Edinburgh, Scotl Conference Date: 19890313
Sponsor: IEEE, Electron Devices Soc, New York, NY, USA; IEE, London, Engl
E.I. Conference No.: 12692
Source: Proc 1989 Int Conf Microelectron Test Struct. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89CH2693-0), Piscataway, NJ, USA. p 245-250
Publication Year: 1989
ISBN: 0-87942-714-0
Language: English

Document Type: PA; (Conference Paper) Treatment: A; (Applications); X; (Experimental)
Journal Announcement: 9002
Abstract: A test structure for detecting the location of the breakdown of a **trench** capacitor electrically is introduced. It is very important to know location of breakdown in order to improve oxide integrity. However, the conventional failure analysis method for a plane capacitor cannot be applied to a **trench** capacitor. A **vertical** n-channel MOS **transistor** is formed in the **trench** . An n-type substrate and surface n-type region are used as source and drain, respectively. The side surface of the **trench** in a p-well acts as a channel region. If the gate potential is lower than the threshold voltage of the n-channel MOSFET, they are electrically separated from each other. The location of oxide breakdown in the **trench** can be detected by checking the leakage current between gate electrode and drain, p-well and source. All capacitors show breakdown at either the bottom or the top of **trench** , not the side. 8 refs.
Descriptors: *CAPACITORS--*Testing; DATA STORAGE, DIGITAL--Random Access; SEMICONDUCTOR DEVICE TESTING
Identifiers: TEST STRUCTURE; **TRENCH** CAPACITOR; BREAKDOWN LOCATION; OXIDE INTEGRITY; **DRAM**
Classification Codes:
714 (Electronic Components); 722 (Computer Hardware)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

6/9/21 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04412486 JICST ACCESSION NUMBER: 00A0066770 FILE SEGMENT: JICST-E
IEDM 99.
KAWANE TOSHIAKI (1)
Gekkan Semiconductor World(Semiconductor World), 1999, VOL.18,NO.12, PAGE.74-75, FIG.2
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: IEDM'99 (Washington D.C. on 12/5-12/9th, 1999)was held. This is a report from the meeting. This time, there was a proposal of the epoch-making **transistor** structure in CMOS device in which the limit for the refinement began to be seen from the viewpoint of power consumption and lithography. It is a **transistor** (VRG MOSFET) of the **vertical** structure in which gate,source and drain are fabricated perpendicularly to the substrate. Lucent Technology reported a **transistor** of the 50nm gate length and Infineon/IBM reported a **vertical transistor** (VERI VEST) for the **DRAM trench** cell.
DESCRIPTORS: **transistor** ; longitudinal type; gate circuit; MOSFET; chemical vapor deposition; **DRAM**
IDENTIFIERS: Lucent Technology; Infineon Technologies; IBM; IEDM99
BROADER DESCRIPTORS: semiconductor device; solid state device; type; circuit; MISFET; FET; vapor deposition; RAM; memory(computer); equipment; dynamic memory
CLASSIFICATION CODE(S): NC03070N
?

```
Set     Items   Description
S1      22510   DRAM OR DYNAMIC()RANDOM()ACCESS()(MEMORY OR MEMORIES)
S2      12903   MC=(U11-C18A3 OR U13-D07)
S3      35103   S1 OR S2
S4     751200   TRENCH? OR GROOVE? OR TRACK?
S5       2875   S4 AND S3
S6      55184   STRAP?
S7         79   S5 AND S6
S8         37   S7 AND TRANSISTOR?
S9         29   S8 AND CAPACITOR?
S10        13   S9 AND VERTICAL?
S11         4   S10 AND PERPENDICULAR?
S12        14   S8 AND DIFFUSION?
S13         5   S12 AND SIDEWALL?
S14        24   S10 OR S12
S15         0   S14 NOT S5
S16        19   S14 NOT S13
S17        15   S16 NOT S11
S18        13   S10 NOT S15
?show files
File 344:CHINESE PATENTS ABS MAY 1985-2002/MAY
         (c) 2002 EUROPEAN PATENT OFFICE
File 347:JAPIO Oct 1976-2002/Feb(Updated 020604)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200239
         (c) 2002  Thomson Derwent
File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
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?ds

Set      Items   Description
S1          35   AU='KAJIYAMA TAKESHI'
S2           0   S1 AND DRAM
S3           0   S1 AND STRAP?
S4           6   S1 AND TRENCH?
?show files
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200239
         (c) 2002  Thomson Derwent
File 347:JAPIO Oct 1976-2002/Feb(Updated 020604)
         (c) 2002 JPO & JAPIO
?
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17/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014350894
WPI Acc No: 2002-171597/200222
XRAM Acc No: C02-053039
XRPX Acc No: N02-130526
Clearing of isolation collar from deep trench **while leaving at other surfaces of deep** trench **, by depositing barrier material and silicon layer, implanting dopant ions, etching the unimplanted silicon, and removing isolation collar**
Patent Assignee: INFINEON TECHNOLOGIES NORTH AMERICA CORP (INFN); INT BUSINESS MACHINES CORP (IBMC)
Inventor: BERGNER W; BRONNER G B; DIVAKARUNI R; GRUENING U; KUDELKA S; MANDELMAN J A; MICHAELIS A; NESBIT L; RADENS C J; SCHLOESSER T; TEWS H H
Number of Countries: 021 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200201607	A2	20020103	WO 2001US20206	A	20010625	200222	B

Priority Applications (No Type Date): US 2000603442 A 20000623
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200201607	A2	E	37	H01L-000/00	

Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Abstract (Basic): WO 200201607 A2
NOVELTY - Clearing of an isolation collar from a first interior surface of a deep **trench** at above storage **capacitor** while leaving the isolation collar at other surfaces of the deep **trench** , comprises depositing a barrier material above a node conductor of storage **capacitor** ; depositing silicon layer; implanting dopant ions; etching the unimplanted silicon; and removing the isolation collar.
DETAILED DESCRIPTION - Clearing of an isolation collar from a first interior surface of a deep **trench** at above a storage **capacitor** while leaving the isolation collar at other surfaces of the deep **trench** , comprises:
(a) depositing a barrier material above a node conductor of the storage **capacitor** ;
(b) depositing silicon layer over the barrier material;
(c) implanting dopant ions at an angle into the layer of deposited silicon within the deep **trench** , to leave the deposited silicon unimplanted along one side of the deep **trench** ;
(d) etching the unimplanted silicon; and
(e) removing the isolation collar in locations previously covered by the unimplanted silicon, leaving the isolation collar in locations covered by the implanted silicon.
USE - For clearing an isolation collar from a first interior surface of a deep **trench** at above a storage **capacitor** while leaving the isolation collar at other surfaces of the deep **trench** .
ADVANTAGE - The method forms the buried **strap** interconnection and **vertical transistor** along the one deep **trench** sidewall, while isolating the other sidewall coincident with the active area pattern. It eliminates spurious **strap** formations, which in turn, drives deep shallow **trench** isolation for sub 8F2 cells. The structure formed by the method can eliminate the need for deep shallow **trench** isolation in all directions. The method and structure also provides lithographic friendly cells and active area definitions for **trench** cells. The method permits buried bit lines stacked **vertical dynamic random access memory** (**DRAM**) cells to have shallow **trench** isolation. It enables high density **DRAM** self-fabrication by selectively removing one side of a collar using angled implantation.
pp; 37 DwgNo 0/28
Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The deposited silicon is undoped. The barrier material comprises nitride. The deposited silicon comprises amorphous silicon. The dopant ions comprise positively charged ions and boron ions.

Preferred Method: The method comprises prefilling the deep **trench** over the barrier material with an oxide; and recessing the oxide in the deep **trench** prior to depositing the silicon layer to reduce an aspect ratio of the deep **trench** . The method further comprises performing an oxidation cycle after implanting the dopant ions to selectively oxidize portions of the silicon layer in which the dopant ions have been implanted; and etching the less oxidized portions of the silicon layer. Removing the isolation collar comprises:

(a) depositing a second barrier layer on the implanted silicon walls of the deep **trench** ;

(b) etching portions of the implanted silicon not having the barrier layer; and

(c) etching an upper portion of the collar.

ORGANIC CHEMISTRY - Preferred Material: The oxide is deposited from a tetraethylorthosilicate precursor

Title Terms: CLEAR; ISOLATE; COLLAR; DEEP; **TRENCH** ; LEAVE; SURFACE; DEEP; **TRENCH** ; DEPOSIT; BARRIER; MATERIAL; SILICON; LAYER; IMPLANT; DOPE; ION; ETCH; SILICON; REMOVE; ISOLATE; COLLAR

Derwent Class: E11; L03; U11

International Patent Class (Main): H01L-000/00

File Segment: CPI; EPI

Manual Codes (CPI/A-N): E05-E03; E31-Q; L04-C02B; L04-C07; L04-C12C

Manual Codes (EPI/S-X): U11-C05F6; U11-C05G1B; U11-C08A3

Chemical Fragment Codes (M3):

01 B414 B713 B720 B831 M210 M212 M272 M283 M320 M411 M424 M510 M520 M530 M540 M620 M782 M904 M905 Q454 R043 R06010-K R06010-M

02 B105 B305 B720 B803 B831 M411 M417 M424 M782 M904 M905 Q454 R043 R11554-K R11554-M

Specific Compound Numbers: R06010-K; R06010-M; R11554-K; R11554-M

Key Word Indexing Terms:

01 1454-0-0-0-CL 132353-0-0-0-CL

17/9/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014268261 **Image available**
WPI Acc No: 2002-088959/200212
XRAM Acc No: C02-027337
XRPX Acc No: N02-065496

Formation of dynamic random access memory **cell includes forming protective layer on** vertical **dielectric layer, depositing conductive material within** trench , **and stripping conductive material and protective layer**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: HARRINGTON J G; HORAK D V; HOULIHAN K M; LAM C H; MIH R D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6326275	B1	20011204	US 2000559363	A	20000424	200212	B

Priority Applications (No Type Date): US 2000559363 A 20000424
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6326275	B1		5	H01L-021/20	

Abstract (Basic): US 6326275 B1

NOVELTY - A **dynamic random access memory** (**DRAM**) cell is formed by:

(a) forming a protective layer (120) on **vertical** dielectric layer above spacer layer;

(b) stripping the spacer layer; and

(c) forming a **strap** layer in place of the spacer layer by depositing a conductive material within a **trench** and stripping both the conductive material and the protective layer.

DETAILED DESCRIPTION - Formation of a **DRAM** cell comprises forming a **trench capacitor** in a silicon substrate having a top dielectric layer (25).

The **trench capacitor** has a top surface which recesses a first distance below the substrate surface.

Vertical silicon walls in a **transistor trench** separate the **capacitor** top surface from the substrate surface.

A **vertical** dielectric layer (110) is formed on the **vertical** walls, and a spacer layer (150) is formed above the **capacitor** top surface within the **transistor trench** .

A protective layer, which is different in composition from the **vertical** dielectric layer and from the spacer layer, is formed on the **vertical** dielectric layer above the spacer layer.

Then, the spacer layer is stripped and a **strap** layer is formed in place of the spacer layer by depositing a conductive material within the **trench** and stripping both the conductive material and the protective layer.

Afterwhich, the **vertical** dielectric layer is stripped and a **vertical** gate dielectric layer is formed on the **vertical** walls.

A conductive wordline material is deposited in the **trench** adjacent the **vertical** gate dielectric, thus forming a gate for a **vertical transistor** .

USE - For forming a **DRAM** cell.

ADVANTAGE - The method avoids the need for extra stripping operation to remove the protective layer. The **trench** wall is preserved against all the reactive ion etching damages during buried **strap** formation.

DESCRIPTION OF DRAWING(S) - The figures show the inventive method.

Top dielectric layer (25)

Vertical dielectric layer (110)

Protective layer (120)

Spacer layer (150)

pp; 5 DwgNo 3, 4/8

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The conductive material and the protective layer are stripped simultaneously. A wordline aperture is further formed in the top dielectric layer for connecting memory cells and making contact with the **trench** .

The conductive wordline material is deposited in the wordline aperture and in the **trench** simultaneously, thus forming a wordline and a set of gates for the **vertical transistors** simultaneously. The top dielectric layer is removed, leaving a projecting portion of the conductive wordline material extending above the substrate.

Sidewalls are formed on the projecting portion of the conductive wordline material and the substrate is implanted forming a first electrode of the **vertical capacitors** .

The substrate is annealed, where dopant diffuses out from the conductive **strap** layer into the substrate such that a second electrode of the **vertical transistors** is formed.

INORGANIC CHEMISTRY - Preferred Materials: The spacer layer is formed from intrinsic polysilicon, the protective layer is formed from doped polysilicon, and the **strap** layer is formed from arsenic-doped polysilicon.

Title Terms: FORMATION; DYNAMIC; RANDOM; ACCESS; MEMORY; CELL; FORMING; PROTECT; LAYER; **VERTICAL** ; DIELECTRIC; LAYER; DEPOSIT; CONDUCTING; MATERIAL; **TRENCH** ; STRIP; CONDUCTING; MATERIAL; PROTECT; LAYER

Derwent Class: L03; U11
International Patent Class (Main): H01L-021/20
International Patent Class (Additional): H01L-021/8242
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C07E; L04-C10A
Manual Codes (EPI/S-X): U11-C01J1; U11-C18B5

17/9/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014241896 **Image available**
WPI Acc No: 2002-062596/200208
XRAM Acc No: C02-017908
XRPX Acc No: N02-046465

Formation of electrical connection to interior plate of trench capacitor **located in deep** trench **on semiconductor substrate involves low-angle implanting dopant into exposed regions of mask layer to create self-aligned mask**

Patent Assignee: INFINEON TECHNOLOGIES NORTH AMERICA CORP (INFN)
Inventor: KUDELKA S; LEE B S; MICHAELIS A; SCHROEDER U; TEWS H H
Number of Countries: 021 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200191180	A2	20011129	WO 2001US15757	A	20010515	200208	B

Priority Applications (No Type Date): US 2000576465 A 20000523
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200191180	A2	E	38	H01L-021/768	

Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Abstract (Basic): WO 200191180 A2

NOVELTY - An electrical connection to an interior plate of a **trench capacitor** located in a deep **trench** on a semiconductor substrate is formed by low-angle implanting a dopant into exposed regions of a mask layer to create a self-aligned mask over the **trench** .

DETAILED DESCRIPTION - Formation of an electrical connection to an interior plate of a **trench capacitor** located in a deep **trench** (104) on a semiconductor substrate (100), includes (a) low-angle implanting a dopant into exposed regions of a mask layer overlying the substrate; (b) removing either the doped exposed regions or the undoped shielded region of the mask using a dopant level selective semiconductor process, thus exposing a first region of the deep **trench** , where a second region of the deep **trench** remains masked; and (c) forming a buried **strap** in the first region of the deep **trench** . The buried **strap** electrically connects the interior plate to a portion of an upper substrate sidewall of the deep **trench** . The mask layer comprises a low-aspect ratio well over the deep **trench** . A shielded region of the mask layer overlying the deep **trench** is shielded from the implanting step by a sidewall of the well and thus remains undoped.

An INDEPENDENT CLAIM is also included for a method of forming a **dynamic random access memory** (**DRAM**) integrated circuit, comprising: forming a storage **capacitor** in the deep **trench** in the substrate; forming an undoped mask layer overlying the substrate; low-angle implanting the dopant into the mask layer; removing either the doped exposed region or the undoped shielded region of the mask using the dopant-level selective semiconductor process, thus exposing a first region of the deep **trench** , where the second region of the deep **trench** remains masked; removing material from the first region of the deep **trench** , thus exposing the upper substrate sidewall of the deep **trench** ; depositing a conductive layer to form the buried **strap** electrically connecting the interior plate to a portion the upper substrate sidewall; and forming a **vertical transistor** on the upper substrate sidewall, where a terminal of the **transistor** is electrically connected to the buried **strap** . The mask layer forms a well with sidewalls over the deep **trench** . The well has a low-aspect height to width ratio.

USE - The method is used for forming an electrical connection to an interior plate of a **trench capacitor** located in a deep **trench** on a semiconductor substrate.

ADVANTAGE - The method provides a **DRAM** memory cell that can be formed with the **trench capacitor** and the **vertical transistor**, thus using devices of manageable size yet occupying horizontal planar area. The buried **strap** and the **vertical trench transistor** may be formed without the use of expensive DUV mask processes. They may be formed with a more robust process than one using a high-angle implantation and high-aspect ratio structure approach. The mask created for use in selective processing of the **trench** is self-aligned with the **trench**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an integrated circuit structure.

Substrate (100)
Collar oxide (106)
Node dielectric (108)
pp; 38 DwgNo 1/24

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Properties: The low-angle is at most 80. The low-aspect ratio is at most 3:1.

Preferred Method: The dopant-level selective semiconductor process is selective oxidation followed by oxide etching; or a selective etch process. The mask layer is oxidized following the selective etch process. The doped exposed regions of the mask layer are removed. The step of forming the storage **capacitor** includes forming a collar oxide (106) on the upper interior surface of the deep **trench**, leaving a lower portion of the deep **trench** uncovered with the collar oxide, forming a first plate in the substrate adjacent the deep **trench**, forming a node dielectric (108) on an interior surface of the deep **trench** and covering the collar oxide, and forming the interior plate on an interior surface of the node dielectric and filling at least a portion of the interior of the deep **trench**. The **vertical transistor** is formed by forming a drain in the substrate adjacent the lower portion of the upper substrate sidewall as the terminal electrically connected to the buried **strap**, forming a **vertical** gate insulator in the **trench** on the upper substrate sidewall, forming a gate in the **trench** adjacent the gate insulator, and forming a source terminal in the substrate adjacent an upper portion of the upper substrate sidewall.

INORGANIC CHEMISTRY - Preferred Component: The mask layer is polysilicon. The implanted dopant is boron, arsenic and/or phosphorus

Title Terms: FORMATION; ELECTRIC; CONNECT; INTERIOR; PLATE; **TRENCH**; **CAPACITOR**; LOCATE; DEEP; **TRENCH**; SEMICONDUCTOR; SUBSTRATE; LOW; ANGLE; IMPLANT; DOPE; EXPOSE; REGION; MASK; LAYER; SELF; ALIGN; MASK

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/768

International Patent Class (Additional): H01L-021/02

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C02B; L04-C13B; L04-C14A

Manual Codes (EPI/S-X): U11-C02B2; U11-C05D3; U11-C05G1B

17/9/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014017469 **Image available**
WPI Acc No: 2001-501683/200155
Related WPI Acc No: 2001-315686
XRPX Acc No: N01-371997

Trench capacitor **type** DRAM **cell has** vertical **metal oxide semiconductor field effect** transistor **transfer device in upper portion of deep** trenches **and collar isolation oxide in upper portion on deep** trench **side walls**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: FURUKAWA T; HAKEY M C; HORAK D V; MA W H; MANDELMAN J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6184549	B1	20010206	US 9886057	A	19980528	200155	B
			US 99296807	A	19990423		

Priority Applications (No Type Date): US 9886057 A 19980528; US 99296807 A 19990423

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6184549	B1		10	H01L-027/108	Div ex application US 9886057

Abstract (Basic): US 6184549 B1

NOVELTY - Deep **trenches** (74,75,74',75') are formed in p type substrate with lower portion partially filled with n+ polysilicon storage node and surrounded by n+ silicon storage plate. **Vertical** MOSFET transfer device is formed in upper portion of **trenches** . A collar isolation oxide is formed in upper portion on deep **trench** side walls between n+ buried **strap diffusion** of MOSFET and storage plate.

DETAILED DESCRIPTION - A recessed polysilicon conductor is provided within upper portion of deep **trenches** gating and p type silicon adjacent deep **trench** . A gate conductor connects an n+ bit line **diffusion** (65) formed above p type silicon and n+ buried **strap diffusion** . Several recessed active and passive wordline conductors are formed on insulating layer above **trenches** .

USE - **Trench capacitor** type integrated circuit **dynamic random access memory** .

ADVANTAGE - Byintegrating robust transfer device in **dynamic random access memory** cell with shallow **trench** isolation region constructed between adjacent **trench capacitor** cells, the device channel length requirement is made independent of cell size, thus the dimension of device can be reduced. Using square printing to form shallow **trench** isolation and detrenches, scaling of the cell to very small dimensions is allowed.

DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of **trench capacitor** type **DRAM** cell.

Line **diffusion** (65)
Deep **trenches** (74,75,74',75')
pp; 10 DwgNo 9/11

Title Terms: **TRENCH** ; **CAPACITOR** ; TYPE; **DRAM** ; CELL; **VERTICAL** ; METAL; OXIDE; SEMICONDUCTOR; FIELD; EFFECT; **TRANSISTOR** ; TRANSFER; DEVICE; UPPER; PORTION; DEEP; **TRENCH** ; COLLAR; ISOLATE; OXIDE; UPPER; PORTION; DEEP; **TRENCH** ; SIDE; WALL
Derwent Class: U13; U14
International Patent Class (Main): H01L-027/108
File Segment: EPI
Manual Codes (EPI/S-X): U13-C04B1A; U14-A03B4

18/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014417653 **Image available**
WPI Acc No: 2002-238356/200229
XRAM Acc No: C02-071889
XRPX Acc No: N02-183623
Fabrication of dynamic random access memory **cell with** vertical transistor **comprises controlling depth of** trench **and forming gate in** trench **to cover surfaces of substrate and shallow** trench **isolation**
Patent Assignee: HEO K (HEOK-I); LIN J (LINJ-I)
Inventor: HEO K; LIN J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010044188	A1	20011122	US 2001854590	A	20010515	200229	B

Priority Applications (No Type Date): TW 2000109310 A 20000516
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010044188	A1		19	H01L-021/8238	

Abstract (Basic): US 20010044188 A1

NOVELTY - A memory cell with **vertical transistor** is fabricated by forming gate in **trench** to cover surfaces of substrate and shallow **trench** isolation; and forming source and drain regions perpendicularly to each other. The depth of **trench** and location of gate are controlled to avoid overlap of source and drain regions.

DETAILED DESCRIPTION - Fabricating memory cell with **vertical transistor** comprises forming a pad layer on the surface of a semiconductor substrate (200). A deep **trench** is formed in the substrate. A **trench capacitor** is formed at the lower portion of the deep **trench** . A collar oxide layer (214) is formed on sidewalls of the upper portion of the deep **trench** that is above the **trench capacitor** .

A first conductive layer (216) formed above the **trench capacitor** fills the deep **trench** . The first conductive layer is etched to a first predetermined depth in the deep **trench** to form a first opening. A portion of the collar oxide layer is removed above the first conductive layer.

A second conductive layer is formed to fill the first opening. The second conductive layer is etched back to a second predetermined depth to form a second opening where the residual second conductive layer forms a buried **strap** (220').

A first insulating layer (222) is formed conformally over the pad layer and the sidewalls and bottom of the second opening.

A second masking layer is formed over the first insulating layer so that the second masking layer fills the inner space of the second opening.

A planarization process is performed to remove portions of the second masking layer and the first insulating layer above the pad layer. The pad layer, substrate, second masking layer, first insulating layer, collar oxide layer, and first conductive layer are defined to a third predetermined depth to form a third opening.

A second insulating layer is formed to fill the third opening. A portion of the second insulating layer is removed to form a shallow **trench** isolation (252). A portion of the second masking layer is removed to a fourth predetermined depth and a fourth opening is formed. The pad layer is removed to expose the surface of the substrate.

A third insulating layer is formed on the exposed surface of the substrate and the surface of the second masking layer in the fourth opening. A well (246) is formed at the upper portion of the substrate. The third insulating layer and the first insulating layer covering the substrate in the fourth opening are removed while the residual first insulating layer and the second masking layer are left on the buried **strap** .

The second masking layer is removed on the bottom of the fourth opening.

A fourth insulating layer is formed on the surface of the substrate and on the sidewalls of the fourth opening. The portion of the fourth insulating layer on the top surface of the substrate is removed to form a gate oxide (260).

A third conductive layer and a fourth conductive layer are sequentially formed to fill the fourth opening and cover the surface of both substrate and shallow **trench** isolation. The third conductive layer and the fourth conductive layer are defined to form a gate (270).

Finally, source (282) and drain (280) regions and gate spacers (290) are formed.

USE - For fabricating a memory cell, i.e., **dynamic random access memory** (**DRAM**) cell, with **vertical transistor** .

ADVANTAGE - The method prevents the drain region and the source region from short-circuiting.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of partially fabricated integrated circuit structure at a stage in forming a **vertical transistor** of a **DRAM** cell of the invention.

Substrate (200)
Collar oxide layer (214)
First conductive layer (216)
Buried **strap** (220')
First insulating layer (222)
Well (246)
Shallow **trench** isolation (252)
Gate oxide (260)
Gate (270)
Drain (280)
Source (282)
Gate spacers (290)
pp; 19 DwgNo 2R/2

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The semiconductor substrate is a silicon substrate. The pad layer is a pad nitride layer or a pad oxide layer. Each conductive layer is polysilicon doped with arsenic ions or phosphorus ions. It has a thickness of 2500-4000 Angstrom. The first predetermined depth is 2500-5500 Angstrom beneath the surface of the substrate. The second predetermined depth is 2000-5000 Angstrom beneath the surface of the substrate. The third predetermined depth is 3000-6000 Angstrom beneath the substrate surface. The fourth predetermined depth is 2000-5000 Angstrom beneath the substrate surface. The first insulating layer is composed of high density plasma (HDP) oxide having a thickness of 250-650 Angstrom. The second masking layer is a polysilicon layer having a thickness of 2500-4000 Angstrom. The second insulating layer is an oxide layer or HDP oxide layer having a thickness of 4000-7000 Angstrom. The third insulating layer is a thermal oxide layer formed by rapid thermal oxidation to a thickness of 50-150 Angstrom. The fourth insulating layer is a thermal oxide having a thickness of 50-150 Angstrom. The third conductive layer is doped polysilicon having a thickness of 650-1000 Angstrom. The fourth conductive layer has a thickness of 500-9020 Angstrom.

Title Terms: FABRICATE; DYNAMIC; RANDOM; ACCESS; MEMORY; CELL; **VERTICAL** ; **TRANSISTOR** ; COMPRISE; CONTROL; DEPTH; **TRENCH** ; FORMING; GATE; **TRENCH** ; COVER; SURFACE; SUBSTRATE; SHALLOW; **TRENCH** ; ISOLATE

Derwent Class: L03; U11; U14

International Patent Class (Main): H01L-021/8238

International Patent Class (Additional): H01L-021/336; H01L-021/8242

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C11C1; L04-E01

Manual Codes (EPI/S-X): **U11-C18A3** ; U11-C18B5; U14-A03B4

18/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014417654 **Image available**
WPI Acc No: 2002-238357/200229
XRAM Acc No: C02-071890
XRPX Acc No: N02-183624
Memory cell fabrication for dynamic random access memory **(** DRAM **) including formation of** vertical transistor **in** trench **to prevent short circuiting of drain and source region**
Patent Assignee: NAN YA TECHNOLOGY CORP (NANY-N); HEO K (HEOK-I); LIN J (LINJ-I); NANYA TECHNOLOGY CORP (NANY-N)
Inventor: HE K; LIN J; HEO K
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010044189	A1	20011122	US 2001854696	A	20010515	200229 B
US 6355529	B2	20020312	US 2001854696	A	20010515	200229
TW 451425	A	20010821	TW 2000109309	A	20000516	200239

Priority Applications (No Type Date): TW 2000109309 A 20000516
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010044189	A1		17	H01L-021/336	
US 6355529	B2			H01L-021/8242	
TW 451425	A			H01L-021/8242	

Abstract (Basic): US 20010044189 A1
NOVELTY - Memory cell fabrication includes the formation of a **vertical transistor** in a **trench** instead of on the substrate surface such that the gate is located in the **trench** and extends to the substrate surface and the STI. The source and drain regions are formed perpendicular to each other and do not overlap.
DETAILED DESCRIPTION - Fabrication comprises:
(a) forming a pad layer (207) on a substrate surface (204);
(b) forming a deep **trench** in the substrate (200) and forming a **trench capacitor** in the lowest part;
(c) forming a collar oxide layer on the **trench** sidewalls above the **capacitor** ;
(d) filling the **trench** with a conductive layer above the **capacitor** and removing part of it to form an opening;
(d) removing part of the collar oxide layer until the top of the oxide layer is lower than the top of the conductive layer;
(e) filling the 1st opening with a 2nd conductive layer;
(f) forming a 2nd opening and filling with a 1st insulating layer to form a shallow **trench** isolation (STI);
(g) partially removing the 2nd conductive layer to form a buried **strap** and a 3rd opening;
(h) forming insulating spacers on the sidewalls of the 3rd opening and forming a 2nd insulating layer on the buried **strap** ;
(i) removing the pad layer and the insulating spacer;
(j) forming a 3rd insulating layer on the exposed substrate and the sidewalls of the 3rd opening;
(k) forming a well at the upper part of the substrate;
(l) removing the 3rd insulating layer and forming a 4th insulating layer on the well;
(m) removing the 4th insulating layer on the top of the well to form a gate oxide;
(n) forming 3rd and 4th conductive layers to fill the 3rd opening and cover the surface of the substrate and STI; then
(o) forming gate, source and drain regions, and gate spacers.
USE - DRAMs with **vertical transistor** .
ADVANTAGE - Short circuiting is prevented between the source and drain regions.
DESCRIPTION OF DRAWING(S) - The diagram shows a cross-section of the semiconductor substrate at the start of processing.

Substrate (200)
Pad oxide layer (202)
Substrate surface (204)
Pad nitride layer (206)
Masking layer (208)
pp; 17 DwgNo 2A/2

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Materials: The substrate is made of silicon. The pad layer is formed of a pad nitride (206) layer and a pad oxide layer (202. The 1st and 2nd conductive layers have a thickness of 2,500-4,000 Angstroms and are made of polysilicon doped with arsenic ions or phosphorus ions. The 3rd conductive layer is of doped polysilicon. The 1st insulating layer is made of a high density plasma oxide and is 4,000-7,000 Angstroms thick. The spacers are made of silicon nitride. The 2nd, 3rd and 4th insulating layers are thermal oxides made by thermal oxidation process.

Preferred Structure: The 1st opening is 2,400-5,500 Angstroms thick, the 2nd opening is 3,000-6,000 Angstroms deep and the 3rd opening is 2,000-5,000 Angstroms thick. The 1st conductive layer is 2,500-4,000 Angstroms thick, the 2nd conductive layer is 2,500-4,000 Angstroms thick, the 3rd conductive layer is 650-1,000 Angstroms thick and the 4th conductive layer is 500-900 Angstroms thick. The 1st insulating layer is 4,000-7,000 Angstroms thick, the 2nd insulating layer is 300-600 Angstroms thick, the 3rd insulating layer is 50-150 Angstroms thick and the 4th insulating layer is 50-150 Angstroms thick.

Title Terms: MEMORY; CELL; FABRICATE; DYNAMIC; RANDOM; ACCESS; MEMORY; **DRAM** ; FORMATION; **VERTICAL** ; **TRANSISTOR** ; **TRENCH** ; PREVENT; SHORT; CIRCUIT; DRAIN; SOURCE; REGION

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/336; H01L-021/8242

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-E01A

Manual Codes (EPI/S-X): **U11-C18A3**

?t s18/9/1-13

18/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014434048 **Image available**
WPI Acc No: 2002-254751/200230
XRAM Acc No: C02-076033
XRPX Acc No: N02-196827
Trench capacitor **production involves depositing conformal layer in trench , roughening conformal layer surface, forming insulator layer outwardly from roughened layer, and forming polycrystalline plate**
Patent Assignee: AHN K Y (AHNK-I); FORBES L (FORB-I); GEUSIC J E (GEUS-I)
Inventor: AHN K Y; FORBES L; GEUSIC J E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010035549	A1	20011101	US 9810729	A	19980122	200230	B
			US 99467992	A	19991220		

Priority Applications (No Type Date): US 9810729 A 19980122; US 99467992 A 19991220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010035549	A1		12	H01L-027/108	Div ex application US 9810729 Div ex patent US 6025225

Abstract (Basic): US 20010035549 A1

NOVELTY - A **trench capacitor** is formed by forming a **trench** (620) in a substrate (616), depositing a conformal layer in the **trench** , roughening the surface of the conformal layer, forming an insulator layer outwardly from the roughened conformal layer (618), and forming a polycrystalline semiconductor plate outwardly from the insulator layer in the **trench** .

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(A) the production of a memory cell by forming a **transistor** having first and second source/drain regions (604, 608), a body region (606) and a gate (610) in a layer of semiconductor material on a substrate and coupling a **trench capacitor** (614) to one of the source/drain regions of the **transistor ;**

(B) a memory cell comprising a lateral **transistor** (602) and a **trench capacitor ;** and

(C) a memory device comprising an array of memory cells, bit lines each coupled to the memory cells at a first source/drain region of the access **transistor** , word lines disposed orthogonal to the bit lines and coupled to gates of access **transistors** , and row decoder coupled to the word lines and a column decoder coupled to the bit lines to access the array of cells.

USE - For forming a **trench capacitor** for use in high-density circuits, e.g. **dynamic random access memories** .

ADVANTAGE - The **trench capacitor** has an increased surface area compared to conventional **capacitors** . No light is needed to create the roughened texture on the surface of the **capacitor** .

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the memory cell.

Lateral **transistor** (602)
First and second source/drain regions (604, 608)
Body region (606)
Gate (610)
Trench capacitor (614)
Substrate (616)
Roughened conformal layer (618)
Trench (620)
Strap (630)
pp; 12 DwgNo 6/7

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The conformal layer is deposited by depositing amorphous silicon and heating the amorphous silicon to form a polysilicon layer of same conductivity as the adjacent substrate. The surface of the conformal layer is roughened by phosphoric acid etching or anodic etching. A **strap** (630) is formed from the polycrystalline plate to the first source/drain region. The insulator layer is formed by growing an oxide layer outwardly from the roughened conformal layer.

Preferred Components: The first and second source/drain regions of the **transistor** are **vertically** aligned with the body region. The **trench** for the **capacitor** is adjacent to the first source/drain region. The polycrystalline plate comprises polysilicon. A second plate of the **trench capacitor** comprises heavily doped p-type silicon substrate.

Title Terms: **TRENCH** ; **CAPACITOR** ; PRODUCE; DEPOSIT; CONFORM; LAYER; **TRENCH** ; ROUGH; CONFORM; LAYER; SURFACE; FORMING; INSULATE; LAYER; OUTWARD; ROUGH; LAYER; FORMING; POLYCRYSTALLINE; PLATE

Derwent Class: L03; U11; U12; U13; U14

International Patent Class (Main): H01L-027/108

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C10B; L04-C12; L04-E01

Manual Codes (EPI/S-X): U11-C05G1B; U12-C02; U13-C04B1A; U14-A03B4

t s8/9/1,3,4,5,6,7,8,9

8/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014507011 **Image available**
WPI Acc No: 2002-327714/200236
XRAM Acc No: C02-094644
XRPX Acc No: N02-256999
Formation of trench **capacitor in** dynamic random access memory **cell involves forming second** trench **pattern larger than a first** trench **pattern, etching upper masking layer, and implanting** strap **and rim portion with dopant**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DIVAKARUNI R; HO H L; IYER S; IYER S K; KHAN B A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6340615	B1	20020122	US 99466605	A	19991217	200236	B

Priority Applications (No Type Date): US 99466605 A 19991217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6340615	B1		8	H01L-021/8242	

Abstract (Basic): US 6340615 B1
NOVELTY - A **trench** capacitor is formed in a **dynamic random access memory** cell by forming a second **trench** pattern about and larger than a first **trench** pattern; etching an upper masking layer of a layered masking layer through the second **trench** pattern; and implanting a **strap** and a rim portion with a dopant.
DETAILED DESCRIPTION - Formation of a **trench** capacitor in a **dynamic random access memory** (**DRAM**) cell comprises:
(a) forming a first **trench** pattern in a layered masking layer on a surface of a semiconductor body;
(b) etching a **trench** into the semiconductor body through the first **trench** pattern;
(c) forming a first capacitor plate in the semiconductor body about the **trench** ;
(d) forming a dielectric layer on inner surfaces of the **trench** ;
(e) partially filling the **trench** with semiconductor material to form a capacitor plate (114) within the **trench** ;
(f) forming a dielectric collar (116) in an upper portion of the **trench** ;
(g) partially filling the dielectric collar with the semiconductor material;
(h) removing an upper portion of the dielectric collar above top surface of the semiconductor material;
(i) forming a **strap** (104) on the top surface of the semiconductor material;
(j) forming a second **trench** pattern about and larger than the first **trench** pattern;
(k) etching an upper masking layer of the layered masking layer through the second **trench** pattern, stopping on a lower masking layer of the layered masking layer comprising substantially the same material as the dielectric collar, exposing a pull back region (122) of the substrate disposed about the **trench** and covered by the lower masking layer; and (l) implanting the **strap** and the rim portion with a dopant.
USE - The method is used for forming a **trench** capacitor in a **dynamic random access memory** (**DRAM**).
ADVANTAGE - The method is a simple way of forming low resistance **strap** connections for **trench** capacitor **DRAM** cells.
DESCRIPTION OF DRAWING(S) - The figure shows the **strap** and the exposed area around the **trench** being implanted.
Strap (104)

Capacitor plate (114)
Collar (116)
Pull back region (122)
pp; 8 DwgNo 3B/5
Technology Focus:
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The dielectric collar and the lower masking layer are formed from oxide. The upper masking layer is formed from nitride. Preferred Method: The **strap** and the rim portion are implanted with dopant at a non-zero angle with respect to a **vertical** axis, where dopants are implanted directly into the inner surfaces of the **trench** .
INORGANIC CHEMISTRY - Preferred Material: The **strap** is formed from amorphous silicon.
Title Terms: FORMATION; **TRENCH** ; CAPACITOR; DYNAMIC; RANDOM; ACCESS; MEMORY; CELL; FORMING; SECOND; **TRENCH** ; PATTERN; LARGER; FIRST; **TRENCH** ; PATTERN; ETCH; UPPER; MASK; LAYER; IMPLANT; **STRAP** ; RIM; PORTION; DOPE
Derwent Class: L03; U11; U12; U13; U14
International Patent Class (Main): H01L-021/8242
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C02B; L04-C07E; L04-C12; L04-C14A
Manual Codes (EPI/S-X): U11-C05G1B; U11-C18B5; U12-C02A1; U13-C04B1A; U14-A03B4

8/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014417655 **Image available**
WPI Acc No: 2002-238358/200229
XRAM Acc No: C02-071891
XRPX Acc No: N02-183625
Fabrication of memory cell, e.g. dynamic random access memory **cell (DRAM), with** trench **capacitor and** vertical **transistor preventing short circuiting between source and drain**
Patent Assignee: HEO K (HEOK-I); LIN J (LINJ-I)
Inventor: HEO K; LIN J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010044190	A1	20011122	US 2001854698	A	20010515	200229	B

Priority Applications (No Type Date): TW 2000109311 A 20000516
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010044190	A1		15	H01L-021/00	

Abstract (Basic): US 20010044190 A1
NOVELTY - Fabrication of the memory cell comprises forming a **vertical** transistor in the **trench** instead of the substrate surface such that the gate is located in the **trench** and extends to the substrate surface and shallow **trench** isolation (STI). The source and drain are perpendicular to each other and do not overlap.
DETAILED DESCRIPTION - Fabrication comprises:
(a) forming a pad layer (207) on the semiconductor substrate (204) and a deep **trench** in the substrate;
(b) forming a **trench** capacitor in the bottom of the **trench** , forming a collar oxide layer on the sidewalls above the capacitor and filling the rest of the **trench** with a 1st conductive layer;
(c) etching the conductive layer to a depth in the deep **trench** to form a 1st opening;
(d) removing part of the collar oxide layer above the 1st conductive layer and filling the 1st opening with a 2nd conductive layer;
(e) planarising to remove the 2nd conductive layer over the pad layer and patterning the pad layer, substrate, 2nd conductive layer, collar oxide layer and 1st conductive layer to form a 2nd opening;

(f) forming a 1st insulating layer on the pad layer and 2nd conductive layer to fill the 2nd opening;

(g) removing part of the 1st insulating layer to form a shallow **trench** isolation (STI) and removing parts of both sides of the **trench** and 2nd conductive layer to form a 3rd opening in which the residual 2nd conductive layer forms a buried **strap** ;

(i) removing pad layer to expose substrate and forming 2nd insulating layer on buried **strap** and exposed substrate;

(j) forming well at top of substrate and removing 2nd insulating layer;

(k) forming a 3rd insulating layer on substrate and surface of buried **strap** to form a gate oxide;

(l) forming 3rd and 4th conductive layers to fill the 4th opening and to cover the substrate surface and STI;

(m) patterning the 3rd and 4th conductive layers to form a gate; then

(n) forming source and drain regions, and a 4th insulating layer.

USE - **DRAM** manufacture with **vertical** transistor.

ADVANTAGE - Short circuiting between source and drain is prevented.

DESCRIPTION OF DRAWING(S) - The diagram shows a cross-section of a semiconductor substrate at the start of the process.

Substrate (200)
Pad oxide layer (202)
Substrate surface (204)
Pad nitride layer (206)
1st masking layer (208)
pp; 15 DwgNo 2A/2

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Materials: The substrate is made of silicon. the pad layer is made of a pad nitride layer (206) and a pad oxide layer (202). The 1st and 2nd conductive layers are formed of polysilicon doped with arsenic or phosphorus ions. The 1st insulating layer is formed of a high density plasma oxide layer. The 2nd and 3rd insulating layers are formed of thermal oxides formed by rapid thermal oxidation. The 4th insulating layer is of silicon nitride.

Preferred Dimensions: The 1st and 2nd conductive layers have a thickness of 2,500-4,000 Angstroms, the 3rd conductive layer has a thickness of 650-1,000 Angstroms and the 4th conductive layer has a thickness of 500-900 Angstroms. The 1st opening has a depth of 2,500-5,500 Angstroms, the 2nd opening has a depth of 3,000-6,000 Angstroms and the 3rd opening has a depth of 2,000-5,000 Angstroms. The 1st insulating layer has a thickness of 4,000-7,000 Angstroms, the 2nd insulating layer has a thickness of 50-150 Angstroms, the 3rd insulating layer has a thickness of 50-150 Angstroms and the 4th insulating layer has a thickness of 200-450 Angstroms.

Title Terms: FABRICATE; MEMORY; CELL; DYNAMIC; RANDOM; ACCESS; MEMORY; CELL ; **DRAM** ; **TRENCH** ; CAPACITOR; **VERTICAL** ; TRANSISTOR; PREVENT; SHORT; CIRCUIT; SOURCE; DRAIN
Derwent Class: L03; U11; U13
International Patent Class (Main): H01L-021/00
International Patent Class (Additional): H01L-021/336; H01L-021/337; H01L-021/338; H01L-021/8238; H01L-021/84
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C06; L04-C10G; L04-C12C; L04-C14A; L04-E01A
Manual Codes (EPI/S-X): U11-C18A3; U13-D07

8/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014417654 **Image available**
WPI Acc No: 2002-238357/200229
XRAM Acc No: C02-071890
XRPX Acc No: N02-183624

17/9/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012946797 **Image available**
WPI Acc No: 2000-118647/200011
XRAM Acc No: C00-036589
XRPX Acc No: N00-089934
Controlling trench **isolation layer thickness in semiconductor memories**
Patent Assignee: SIEMENS AG (SIEI); INFINEON TECHNOLOGIES AG (INFN)
Inventor: GRUENING U
Number of Countries: 030 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 977256	A2	20000202	EP 99113538	A	19990706	200011	B
JP 2000058778	A	20000225	JP 99214006	A	19990728	200021	
CN 1244036	A	20000209	CN 99111868	A	19990730	200026	
US 6074909	A	20000613	US 98127262	A	19980731	200035	
KR 2000012124	A	20000225	KR 9931507	A	19990731	200102	
TW 425654	A	20010311	TW 99112385	A	19990721	200143	
US 6359299	B1	20020319	US 98127262	A	19980731	200224	
			US 2000503992	A	20000214		

Priority Applications (No Type Date): US 98127262 A 19980731; US 2000503992 A 20000214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 977256	A2	E	18	H01L-021/8242	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000058778	A		11	H01L-027/108	
CN 1244036	A			H01L-021/76	
US 6074909	A			H01L-021/8242	
KR 2000012124	A			H01L-021/283	
TW 425654	A			H01L-021/76	
US 6359299	B1			H01L-027/108	Div ex application US 98127262

Abstract (Basic): EP 977256 A2
NOVELTY - **Trench** isolation layer thickness in a semiconductor memory is controlled by depositing a mask layer to mask isolation material formed over a buried **strap** in the **trench** and remaining exposed isolation.
DETAILED DESCRIPTION - The method comprises:
(a) forming a deep **trench** containing a storage node having a buried **strap** (30);
(b) depositing an isolation layer (28) on the buried **strap** ;
(c) adding a masking layer to cover the isolation formed over the **strap** ; and
(d) removing all isolation material not covered by the mask. The isolation layer is preferably 20 - 50 nm oxide or nitride layer and the masking material is preferably polysilicon.
An INDEPENDENT CLAIM is also included for a method for fabricating vertical **transistors** by recessing a substrate to permit increased overlap between a **transistor** channel and buried **strap** out **diffusion** when the **transistor** is formed.
USE - In fabrication of memories such as **dynamic random access memory** (**DRAM**) cells.
ADVANTAGE - Control of the isolation layer thickness is improved.
DESCRIPTION OF DRAWING(S) - The drawings show cross-sectional views of the semiconductor device at different stages in the fabrication process.
Isolation layer (28)
Buried **strap** (30)
pp; 18 DwgNo 2,5/20
Title Terms: CONTROL; **TRENCH** ; ISOLATE; LAYER; THICK; SEMICONDUCTOR; MEMORY
Derwent Class: L03; U11; U12; U13; U14

International Patent Class (Main): H01L-021/283; H01L-021/76; H01L-021/8242
; H01L-027/108
International Patent Class (Additional): H01L-021/8239
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C06; L04-C12C
Manual Codes (EPI/S-X): U11-C05G1B; U11-C08A3; U12-C02A1; U13-C04B1A;
U14-A03B4

17/9/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011501654
WPI Acc No: 1997-479568/199744
Related WPI Acc No: 1996-370650
XRPX Acc No: N97-400024
Buried strap **for storage** trench **capacitor in** DRAM **- connects capacitor to one of source-drain regions of transfer gate** transistor , **part of buried** strap **comprises recrystallised silicon**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); SIEMENS AG (SIEI); TOSHIBA KK (TOKE)
Inventor: HAMMERL E; HO H L; MANDELMAN J A; SHIOZAWA J; STENGL R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5670805	A	19970923	US 95412442	A	19950329	199744	B
			US 96643983	A	19960507		

Priority Applications (No Type Date): US 95412442 A 19950329; US 96643983 A 19960507
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5670805	A			H01L-027/108	Div ex application US 95412442 Div ex patent US 5543348

Abstract (Basic): US 5670805 A
The device includes a **trench** formed in a semiconductor substrate. Conductive material is formed in the **trench** and is insulatively spaced from the semiconductor substrate to form a capacitor.
A transfer gate **transistor** includes source/drain regions formed on a surface of the semiconductor substrate and a control gate which is insulatively spaced from a channel region between the source and drain regions. A buried **strap** electrically connects the capacitor to one of the source/drain regions of the transfer gate **transistor** . A portion of the buried **strap** includes recrystallised silicon.
ADVANTAGE - Allows manufacture of **diffusion** limiting interconnection between polysilicon fill of deep **trench** capacitor and semiconductor substrate before buried **strap** is out-diffused.
Title Terms: BURY; **STRAP** ; STORAGE; **TRENCH** ; CAPACITOR; **DRAM** ; CONNECT; CAPACITOR; ONE; SOURCE; DRAIN; REGION; TRANSFER; GATE; **TRANSISTOR** ; PART ; BURY; **STRAP** ; COMPRISE; RECRYSTALLISATION; SILICON
Derwent Class: U11; U13; U14
International Patent Class (Main): H01L-027/108
International Patent Class (Additional): H01L-029/76; H01L-029/94
File Segment: EPI
Manual Codes (EPI/S-X): U11-C05D3; U13-C04B1A; U14-A03B4
?

?t s17/9/11-15

17/9/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010873699 **Image available**
WPI Acc No: 1996-370650/199637
Related WPI Acc No: 1997-479568
XRAM Acc No: C96-117543
XRPX Acc No: N96-311860
Method for coupling capacitor and transistor **- comprising forming** trench **in semiconductor substrate, forming impurity-doped conductive region by filling** trench **with conductive material, etc.**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); SIEMENS AG (SIEI); TOSHIBA KK (TOKE); IBM CORP (IBMC)
Inventor: HAMMERL E; HO H L; MANDELMAN J A; SHIOZAWA J; STENGL R J
Number of Countries: 009 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5543348	A	19960806	US 95412442	A	19950329	199637	B
EP 739033	A2	19961023	EP 96105064	A	19960329	199647	
TW 290724	A	19961111	TW 96104692	A	19960419	199711	
JP 9092799	A	19970404	JP 9676252	A	19960329	199724	
KR 202278	B1	19990615	KR 969303	A	19960329	200061	

Priority Applications (No Type Date): US 95412442 A 19950329
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5543348	A		16	H01L-021/8242	
EP 739033	A2	E	16	H01L-021/8242	
Designated States (Regional): DE FR GB IE IT					
TW 290724	A			H01L-021/70	
JP 9092799	A		11	H01L-027/108	
KR 202278	B1			H01L-027/108	

Abstract (Basic): US 5543348 A

Forming a coupled capacitor and **transistor** comprises: (a) forming a **trench** in a semiconductor substrate; (b) forming an impurity-doped first conductive region by filling the **trench** with an impurity-doped first conductive material; (c) back etching the impurity-doped first conductive region to a first level within the **trench** ; (d) forming an insulating layer on a side wall of the portion of the **trench** opened by the back etching; (e) forming a second conductive region by filling the remainder of the **trench** with a second conductive material; (f) back etching the insulating layer and the second conductive material to a second level within the **trench** ; (g) forming an undoped amorphous Si layer in the portion of the **trench** opened by the etching back of the insulating layer and the second conductive region; (h) back etching the undoped amorphous Si layer to a third level within the **trench** ; (i) recrystallising the amorphous Si layer; (j) diffusing out impurities from the impurity-doped first conductive region to the semiconductor substrate through the recrystallised Si layer; (k) forming a source/drain region of the **transistor** adjacent to an intersection of the **trench** and the surface of the substrate, the diffused out impurities and the recrystallised Si layer constituting a buried **strap** for electrically connecting the first and second conductive layers in the **trench** to the source/drain region.

USE - The method is used for forming a buried **strap** for electrically connecting a storage **trench** capacitor to a **transistor** gate in a **trench** -capacitor type **DRAM** cell.

ADVANTAGE - A buried **strap** recrystallisation step allows a much higher thermal budget of the fabrication process to be used for appropriate stress relief anneals without any excessive dopant out-**diffusion** from the **trench** .

Dwg.7A/7

Title Terms: METHOD; COUPLE; CAPACITOR; **TRANSISTOR** ; COMPRISE; FORMING; **TRENCH** ; SEMICONDUCTOR; SUBSTRATE; FORMING; IMPURE; DOPE; CONDUCTING; REGION; FILL; **TRENCH** ; CONDUCTING; MATERIAL
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/70; H01L-021/8242; H01L-027/108
International Patent Class (Additional): H01L-021/225; H01L-021/74; H01L-021/822; H01L-027/04
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C02; L04-C03; L04-C10B; L04-C12; L04-C14A

17/9/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010664964 **Image available**
WPI Acc No: 1996-161918/199617
XRAM Acc No: C96-051303
XRPX Acc No: N96-135624
Dynamic random access memory **cell formation - comprises doping silicon-on-insulator substrate to first conductivity type, forming silicon-on-insulator oxide layer on substrate, etc**
Patent Assignee: SIEMENS AG (SIEI)
Inventor: ALSMEIER J; STENGL R J
Number of Countries: 010 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 703625	A2	19960327	EP 95114657	A	19950918	199617	B
JP 8111513	A	19960430	JP 95248017	A	19950926	199627	
TW 288203	A	19961011	TW 95113512	A	19951218	199708	
US 5627092	A	19970506	US 94313507	A	19940926	199724	

Priority Applications (No Type Date): US 94313507 A 19940926
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 703625	A2	E	17	H01L-027/108	
Designated States (Regional): AT DE FR GB IE IT NL					
JP 8111513	A		10	H01L-027/108	
US 5627092	A		15	H01L-021/70	
TW 288203	A			H01L-027/108	

Abstract (Equivalent): US 5627092 A

A method for forming a **dynamic random access memory** cell (**DRAM**), comprising the steps of: doping a silicon on isolator (SOI) substrate with dopants of a first conductivity type; forming an SOI oxide layer on the substrate; forming a silicon device layer over the SOI oxide layer; doping the silicon device layer with dopants of a second conductivity type opposite that of the first conductivity type; forming a pad nitride layer over the silicon device layer; forming a TEOS etch mask layer over the pad nitride layer; etching a **trench** into the substrate at a first region of it; forming a dielectric layer on interior walls of the **trench** ; filling the **trench** to the top level of the TEOS etch mask layer with a polysilicon material doped to the first conductivity type; removing the TEOS etch mask layer; recess etching the polysilicon material down to about the mid-level of the SOI oxide layer; isotropic etching away the dielectric layer from end portions of the silicon device layers; refilling the **trench** with intrinsic polysilicon material above the remaining first conductivity type doped polysilicon material; recess etching the intrinsic polysilicon material down to about the middle of the silicon device layer, thereby leaving a polysilicon stud protruding from the **trench** ; etching away the pad nitride layer and the silicon device layer on one side of the **trench** , using the associated portion of the SOI oxide layer as an etch stop; thermally oxidizing the polysilicon stud, while permitting out **diffusion** of dopant material from the underlying doped polysilicon material, into and through a remaining portion of initially intrinsic polysilicon material, into an adjacent portion of the silicon device layer on an opposite side of the **trench** for providing a buried **strap** ; chemical vapor depositing (CVD) an oxide layer over the polysilicon stud and the SOI layer adjacent the one side of the **trench** to above the top level of the silicon device layer adjacent the opposite side of the **trench** ; planarising the CVD oxide to the level of the remaining portion of the silicon device layer; oxidizing the silicon device layer with gate sacrificial oxide; and implanting an MOS **transistor** switch including adjacent drain, channel, and source regions in the silicon device layer, with a gate stack consisting of a first gate layer of the first conductivity overlying the channel region, and portions of the drain and source regions, and an intrinsic

second gate layer overlying the first gate layer.
Dwg.4.9/4.
9

Title Terms: DYNAMIC; RANDOM; ACCESS; MEMORY; CELL; FORMATION; COMPRISE; DOPE; SILICON; INSULATE; SUBSTRATE; FIRST; CONDUCTING; TYPE; FORMING; SILICON; INSULATE; OXIDE; LAYER; SUBSTRATE

Derwent Class: L03; U13; U14

International Patent Class (Main): H01L-021/70; H01L-027/108

International Patent Class (Additional): H01L-021/82; H01L-021/8242; H01L-027/00; H01L-029/786

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C02; L04-C06A; L04-C07E; L04-C10B; L04-C12A; L04-C12B

Manual Codes (EPI/S-X): U13-C04B1A; U13-D03A; **U13-D07** ; U14-A03B4

17/9/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010058464 **Image available**
WPI Acc No: 1994-326175/199441
XRPX Acc No: N94-256219

Memory cell with polysilicon surface strap **in** DRAM **- has electrically conductive** diffusion **barrier between self-aligned horizontal** strap , **coupling storage** trench **to access** transistor diffusion **region, and** diffusion **region**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: RAJEEVAKUMAR T V; SANDA P N
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 621632	A1	19941026	EP 94105556	A	19940411	199441	B
JP 6326269	A	19941125	JP 9477069	A	19940415	199507	
TW 241392	A	19950221	TW 94102537	A	19940323	199518	

Priority Applications (No Type Date): US 9352330 A 19930422
Cited Patents: 04Jnl.Ref; EP 462576; EP 489257; JP 60072261
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 621632	A1	E	13	H01L-021/82	
Designated States (Regional): DE FR GB					
JP 6326269	A		8	H01L-027/108	
TW 241392	A			H01L-027/108	

Abstract (Basic): EP 621632 A

The memory cell includes a self-aligned **strap** pref. a surface **strap** coupling a storage **trench** , in a semiconductor substrate, to a **diffusion** region of an access **transistor** . The **strap** includes an electrically conductive liner **diffusion** barrier material. Pref. the **strap** extends along the substrate horizontal surface and is horizontally self-aligned with the **diffusion** region.

The **strap** may be polysilicon, withe the **diffusion** barrier e.g. TiN or TaN between the polysilicon and the **diffusion** region. The **strap** is pref. self-aligned with a cell word line and with a gate region in the **diffusion** region.

USE/ADVANTAGE - E.g. in 256Mb **DRAM** . Avoids **diffusion strap** ; max. contact area.

Dwg.1/8

Title Terms: MEMORY; CELL; SURFACE; **STRAP** ; **DRAM** ; ELECTRIC; CONDUCTING; **DIFFUSION** ; BARRIER; SELF; ALIGN; HORIZONTAL; **STRAP** ; COUPLE; STORAGE; **TRENCH** ; ACCESS; **TRANSISTOR** ; **DIFFUSION** ; REGION; **DIFFUSION** ; REGION
Index Terms/Additional Words: **TRENC H_CA PACITORMe mory cell w ith polysi licon sur face stra p in D** ; CAPACITOR
Derwent Class: U11; U13
International Patent Class (Main): H01L-021/82
International Patent Class (Additional): H01L-027/108
File Segment: EPI
Manual Codes (EPI/S-X): U11-C05D3; U11-D03B2; U13-C04B1A; U13-D03A

17/9/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009527157 **Image available**
WPI Acc No: 1993-220697/199328
XRPX Acc No: N93-169124
Substrate plate trench DRAM **cell array - uses double well structure which isolates n-channel transfer FETs within separate p-well so that** transistors **operate independently**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: PARK J W; VOLDMAN S H; BRONNER G B; DHONG S H; HWANG W
Number of Countries: 009 Number of Patents: 015
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 550894	A1	19930714	EP 92122009	A	19921224	199328	B
US 5250829	A	19931005	US 92818668	A	19920109	199341	
JP 5283638	A	19931029	JP 92347592	A	19921228	199348	
JP 5283639	A	19931029	JP 92347635	A	19921228	199348	
CN 1076550	A	19930922	CN 93100211	A	19930107	199425	
US 5362663	A	19941108	US 92818668	A	19920109	199444	
			US 9372261	A	19930604		
US 5384474	A	19950124	US 92819159	A	19920109	199510	
			US 93149146	A	19931105		
TW 265477	A	19951211	TW 93102245	A	19930325	199609	
US 5521115	A	19960528	US 92819159	A	19920109	199627	
			US 93149146	A	19931105		
			US 94316693	A	19940930		
SG 45211	A1	19980116	SG 961320	A	19921224	199811	
EP 550894	B1	19990804	EP 92122009	A	19921224	199935	
KR 9704950	B1	19970410	KR 93132	A	19930107	199938	
KR 9704952	B1	19970410	KR 93134	A	19930107	199938	
DE 69229717	E	19990909	DE 629717	A	19921224	199943	
			EP 92122009	A	19921224		
CN 1256519	A	20000614	CN 93100211	A	19930107	200048	
			CN 99118366	A	19930107		

Priority Applications (No Type Date): US 92819159 A 19920109; US 92818668 A 19920109; US 9372261 A 19930604; US 93149146 A 19931105; US 94316693 A 19940930
Cited Patents: US 4967248
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 550894	A1	E	20	H01L-027/108	
Designated States (Regional): DE FR GB					
US 5250829	A		11	H01L-027/02	
JP 5283638	A			H01L-027/108	
JP 5283639	A			H01L-027/108	
CN 1076550	A			H01L-027/108	
US 5362663	A		11	H01L-021/70	Div ex application US 92818668 Div ex patent US 5250829
US 5384474	A		11	H01L-029/78	Cont of application US 92819159
TW 265477	A			H01L-031/042	
US 5521115	A		11	H01L-021/8242	Cont of application US 92819159 Div ex application US 93149146 Div ex patent US 5384474
SG 45211	A1			H01L-027/108	
EP 550894	B1	E		H01L-027/108	
Designated States (Regional): DE FR GB					
KR 9704950	B1			H01L-027/108	
KR 9704952	B1			H01L-027/108	
DE 69229717	E			H01L-027/108	Based on patent EP 550894
CN 1256519	A			H01L-029/78	Div ex application CN 93100211

Abstract (Basic): EP 550894 A
The memory cell includes an n-channel transfer device (14) formed in a p-type well (12) on the upper surface of a p-type semiconductor

substrate (10). Each access **transistor** is coupled to a storage **capacitor** , and has a control electrode (16), a data line contact (18), a diffused n-type storage node region (20) and a channel region.

In fabrication, a storage **capacitor** is formed in a deep **trench** (22) adjacent to the storage node (20) and includes a signal storage node formed by a conductive n-type polysilicon electrode (24) connected to the surface node (20) by a conductive **strap** (26). A thick insulating collar (28) increases the threshold voltage of the **vertical** parasitic FET formed within the p-well. Local surface isolation (30) defines active device regions.

ADVANTAGE - Reduces complexity of design, and provides cell arrays in a simple easy to mfr. processing sequence; reduced charge leakage due to control of parasitic devices.

Dwg.2/19

Abstract (Equivalent): US 5521115 A

The method of making a **dynamic random access memory** device comprising the steps of:

providing a semiconductor substrate of a first conductivity type;

forming a buried region of second conductivity type over at least a portion of the area of said substrate;

forming an array of **trenches** in a matrix pattern in the top surface of said substrate, each **trench** penetrating into said substrate and substantially into said buried region;

forming a dielectric layer of a predetermined thickness on the inside surfaces of said **trenches** and filling said **trenches** with a conductive electrode material;

ion implanting and diffusing around the perimeter of said array of **trenches** a diffused region of said second conductivity type having a depth so as to physically and electrically isolate a portion of the substrate within the matrix pattern above said buried region; and

forming within the isolated portion of the matrix pattern a plurality of semiconductor devices for coupling signals to and from said conductive electrode material within at least some of said **trenches** .

Dwg.10/10

Title Terms: SUBSTRATE; PLATE; **TRENCH** ; **DRAM** ; CELL; ARRAY; DOUBLE; WELL; STRUCTURE; ISOLATE; N-CHANNEL; TRANSFER; FET; SEPARATE; SO; **TRANSISTOR** ; OPERATE; INDEPENDENT

Derwent Class: U11; U13; U14

International Patent Class (Main): H01L-021/70; H01L-021/8242; H01L-027/02; H01L-027/108; H01L-029/78; H01L-031/042

International Patent Class (Additional): G11C-016/00; H01L-021/82; H01L-027/00; H01L-027/04

File Segment: EPI

Manual Codes (EPI/S-X): U11-C18B5; U13-C04B1A; U13-D03A; U14-A03B4

18/9/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009527137 **Image available**
WPI Acc No: 1993-220677/199328
XRPX Acc No: N93-169109
Substrate plate trench capacitor DRAM **cell array - has buried plate electrode in electrically and physically isolated region of substrate so that access** transistors **operate independently from other devices**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: KENNEY D M
Number of Countries: 009 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 550870	A1	19930714	EP 92121739	A	19921221	199328	B
JP 5283640	A	19931029	JP 92347663	A	19921228	199348	
US 5264716	A	19931123	US 92819148	A	19920109	199348	
TW 222716	A	19940421	TW 93100128	A	19930111	199422	
CN 1076310	A	19930915	CN 93100210	A	19930107	199424	
US 5348905	A	19940920	US 92819148	A	19920109	199437	
			US 93112406	A	19930826		
SG 44361	A1	19971219	SG 952309	A	19921221	199808	
KR 9704951	B1	19970410	KR 93133	A	19930107	199938	
CN 1262526	A	20000809	CN 99123542	A	19991111	200055	

Priority Applications (No Type Date): US 92819148 A 19920109; US 93112406 A 19930826
Cited Patents: 01Jnl.Ref; JP 1119057
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 550870	A1	E	15	H01L-027/108	
Designated States (Regional): DE FR GB					
JP 5283640	A			H01L-027/108	
US 5264716	A		12	H01L-027/108	
TW 222716	A			H01L-031/042	
CN 1076310	A			H01L-027/108	
US 5348905	A		14	H01L-021/70	Div ex application US 92819148
					Div ex patent US 5264716
SG 44361	A1			H01L-027/108	
KR 9704951	B1			H01L-027/108	
CN 1262526	A			H01L-027/108	

Abstract (Basic): EP 550870 A
The memory cell includes an n-channel transfer device (14) formed in a p-type well (12) on the upper surface of a p-type semiconductor substrate (10). A control gate (16) couples data between a data or bit line diffused n-type region (18) and a diffused n-type storage node region (20) through the well.
In fabrication, a storage **capacitor** is formed in a deep **trench** (22) adjacent to the access **transistor** storage node (20) and includes a signal storage node formed by a conductive n-type polysilicon electrode (24) connected to the surface node (20) by a conductive **strap** (26). A thick insulating collar (28) increases the threshold voltage of the **vertical** parasitic FET formed within the p-well. Local surface isolation (30) defines active device regions.
ADVANTAGE - Reduces complexity of design, allowing process simplicity and increased yield; high density for e.g. 16Mbit and larger.
Dwg.1/12
Abstract (Equivalent): US 5264716 A
The high density substrate plate **DRAM** cell has a buried plate region formed in an electrically and physically isolated region of the semiconductor substrate, adjacent to deep **trench capacitors** so that the substrate region of **DRAM** transfer FETs is electrically isolated from other FETs on a semiconductor substrate.
The buried region is partially formed by lateral out-diffusion from

the sidewalls of the deep **trenches** and partially formed by an N-well surface diffusion which entirely surrounds the **DRAM** array region.

ADVANTAGE - Minimise charge leakage, optimised device bias.

Dwg.1/12

US 5348905 A

The method comprises of providing a semiconductor substrate of a first conductivity type, and forming a plurality of deep **trenches** in a matrix pattern on a top surface of the substrate. Then diffusing a second conductivity type impurity from the lower portion of the depth of the deep **trenches** into the substrate to form a continuous buried diffused region of a second conductivity type across the entire extent of the matrix pattern. Then forming a dielectric layer on the inside of the deep **trenches** and filling the **trenches** with a conductive electrode material.

Then forming around the perimeter of the matrix pattern a diffused surface region of the second conductivity type having a depth, so as to physically and electrically isolate a portion of the substrate in the matrix pattern above the continuous buried diffused region. Finally forming within the isolated portion of the matrix pattern of semiconductor devices for coupling signals to and from the conductive electrode material in at least some of the deep **trenches** .

ADVANTAGE - Provides a buried plate SPT **DRAM** cell array in which the density limitations of the prior art are removed. Allows process simplicity and thus increased product yield, which has a minimum impact on existing processing technologies.

Dwg.1/12

Title Terms: SUBSTRATE; PLATE; **TRENCH** ; **CAPACITOR** ; **DRAM** ; CELL; ARRAY; BURY; PLATE; ELECTRODE; ELECTRIC; PHYSICAL; ISOLATE; REGION; SUBSTRATE; SO; ACCESS; **TRANSISTOR** ; OPERATE; INDEPENDENT; DEVICE

Derwent Class: U11; U13; U14

International Patent Class (Main): H01L-021/70; H01L-027/108; H01L-031/042

International Patent Class (Additional): H01G-004/06; H01L-021/82; H01L-027/04; H01L-029/00; H01L-029/76

File Segment: EPI

Manual Codes (EPI/S-X): U11-C18B5; U13-C04B1A; U13-D03A; U14-A03B4

17/9/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009181982 **Image available**
WPI Acc No: 1992-309418/199238
XRPX Acc No: N92-236864

DRAM **integrated circuit with floating electrode** capacitor **memory cell - has pair of MOS** transistors **formed on substrate and stack** capacitor **in** trench **between** transistors **and defined by word lines which serve as** transistor **gates with** capacitor **layers extending partly over word lines**

Patent Assignee: SHARP KK (SHAF)
Inventor: ADAN A O
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 503199	A2	19920916	EP 91311823	A	19911219	199238	B
JP 4283963	A	19921008	JP 9148142	A	19910313	199247	
EP 503199	A3	19921104	EP 91311823	A	19911219	199342	
US 5606189	A	19970225	US 91786831	A	19911101	199714	
			US 93111967	A	19930826		
EP 503199	B1	19970409	EP 91311823	A	19911219	199719	
DE 69125593	E	19970515	DE 625593	A	19911219	199725	
			EP 91311823	A	19911219		
KR 251217	B1	20000415	KR 923966	A	19920311	200124	

Priority Applications (No Type Date): JP 9148142 A 19910313
Cited Patents: No-SR.Pub; 6.Jnl.Ref; JP 1018253; JP 1218056; JP 2003274; JP 2297962; US 4958318
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 503199	A2	E	14	H01L-027/108	
Designated States (Regional): DE GB IT NL					
JP 4283963	A		7	H01L-027/108	
EP 503199	A3			H01L-027/108	
US 5606189	A		14	H01L-029/78	Cont of application US 91786831
EP 503199	B1	E	16	H01L-027/108	
Designated States (Regional): DE GB IT NL					
DE 69125593	E			H01L-027/108	Based on patent EP 503199
KR 251217	B1			H01L-027/108	

Abstract (Basic): EP 503199 A

The dynamic RAM memory comprises a pair of N mos **transistors** formed side by side on a p-type substrate (1). A **trench** is formed between adjacent impurity regions (A,B), each at one end of **transistors** . A stack **capacitor** , formed in the **trench** between the adjacent active regions. A first electrode layer (4) of polysilicon connected to one active region (A), a **capacitor** insulating layer (5), and second polysilicon electrode layer (6) connected to the second **transistor** impurity region (B), through a contact **strap** (8).

The layers are formed one over another and are, embedded in **trench** . Pref. the stack **capacitor** extends to partly cover a word line (WL) serving as the gate of each mos **transistor** . In production the **trench** is self registered between the work lines without misalignment.

USE/ADVANTAGE - Increase capacitance with improved reproducibility for three-element, two-bit storage cell. Small area. Increased integration density. Simple mfg. process. 50 per cent cell utility factor.

Dwg.17/23

Abstract (Equivalent): EP 503199 B

A FEC dynamic RAM comprising (a) a pair of capacitively coupled MOS **transistors** (Q1, Q2) formed side by side on a substrate (1'), the first of said pair of MOS **transistors** (Q1) having a source impurity region A and the second of said pair (Q2) having a drain impurity region B, said impurity regions A and B being in adjacent portions of

the respective first and second MOS **transistors** , (b) a **trench** (2) with an insulating layer lining (3) formed in the substrate between said impurity regions A and B, and (c) a stack **capacitor** comprising a first electrode layer (4) connected to the source impurity region A, a **capacitor** insulating layer (5) and a second electrode layer (6) connected to the drain impurity region B through the intermediary of a contact **strap** (8), said layers being formed one over another with said **capacitor** insulating layer sandwiched between said electrode layers, and embedded in said **trench** .

Dwg.1/23

Abstract (Equivalent): US 5606189 A

A two- **transistor** , one- **capacitor** RAM comprising:

(a) said two **transistors** being a pair of capacitively coupled MOS **transistors** formed side by side on a substrate, the first of said pair of MOS **transistors** having a source impurity region A embedded in an upper region of the substrate and the second of said pair having a drain impurity region B embedded in said upper region of the substrate,

(b) a **trench** with an insulating layer lining formed in the substrate between impurity regions A and B adjacent to each other at one end of each of the MOS **transistors** , wherein said **trench** extends below said upper region of said substrate, and

(c) a stack **capacitor** comprising a first electrode layer connected to and overlaying the impurity region A, a **capacitor** insulating layer and a second electrode layer connected to the impurity region B through the intermediary of a contact **strap** , said electrode layers being **vertically** superimposed, sandwiching said **capacitor** insulating layer, and embedded in said **trench** , and being insulated from the substrate by the insulating layer lining in the **trench** ,

wherein a first electrode portion of the first electrode layer overlays a portion of the contact **strap** over impurity region B with an insulating layer therebetween, and the second electrode layer overlays the first electrode portion with an insulating film therebetween.

Dwg.1/23

Title Terms: **DRAM** ; INTEGRATE; CIRCUIT; FLOAT; ELECTRODE; **CAPACITOR** ; MEMORY; CELL; PAIR; MOS; **TRANSISTOR** ; FORMING; SUBSTRATE; STACK; **CAPACITOR** ; **TRENCH** ; **TRANSISTOR** ; DEFINE; WORD; LINE; SERVE; **TRANSISTOR** ; GATE; **CAPACITOR** ; LAYER; EXTEND; WORD; LINE

Index Terms/Additional Words: **DYNA MIC_RAMEP 503199 _A2_H01L -027/1 08 Region al): DE GB IT NL|US** ; RAM

Derwent Class: U11; U13; U14

International Patent Class (Main): H01L-027/108; H01L-029/78

International Patent Class (Additional): H01L-021/82

File Segment: EPI

Manual Codes (EPI/S-X): U11-C18B5; U13-C04B1A; U13-D03A; U14-A03B4

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17/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014416305 **Image available**
WPI Acc No: 2002-237008/200229
XRAM Acc No: C02-071680
XRPX Acc No: N02-182316
Semiconductor device, e.g. dynamic random access memory **device, formed within semiconductor substrate comprises** trench **capacitor, active area having first surface roughened prior to buried** strap **formation, and buried** strap
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: FALTERMEIER J E; FLAITZ P L; HURD J L; JAMMY R; SRINIVASAN R; TRUDEAU F G; WANG Y; WEISS D S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6333531	B1	20011225	US 99239655	A	19990129	200229	B

Priority Applications (No Type Date): US 99239655 A 19990129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6333531	B1		12	H01L-027/108	

Abstract (Basic): US 6333531 B1

NOVELTY - Semiconductor device formed within a semiconductor substrate comprises a **trench** capacitor; active area formed within substrate and having first surface; and buried **strap** formed after active area and including a second surface, and a portion extending from the second surface comprising a high- **diffusion** grain structure. The first surface is roughened prior to formation of buried **strap** .

DETAILED DESCRIPTION - A semiconductor device formed within a semiconductor substrate comprises (1) **trench** capacitor including polycrystalline silicon electrode with dopant impurities; (ii) active area (3) formed within the substrate and having a first surface; and (iii) buried **strap** (15') formed sequentially after the active area and connecting the polycrystalline silicon electrode to the active area. The buried **strap** includes (a) a second surface in confronting relationship with at least the first surface, and (b) at least a portion extending from the second surface comprising a high- **diffusion** grain structure. The first surface is roughened prior to the formation of the buried **strap** .

USE - As semiconductor device, **dynamic random access memory** (**DRAM**) device (claimed).

ADVANTAGE - Improved dopant control can be achieved inn one material by influencing grain growth in an adjacent material. The device provides for a highly diffusive grain structure formed within one material, which enhances **diffusion** of a dopant impurity, and provides for improved dopant control in an adjacent dissimilar material.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a completed semiconductor device.

active area (3)
buried **strap** (15')
pp; 12 DwgNo 7/8

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The high- **diffusion** grain structure is formed in response to nucleation sites formed on the first surface of the active area. The active area includes a portion of the dopant impurities diffused from the polycrystalline silicon electrode and through the polycrystalline silicon adjacent region. It includes an adjacent section adjacent the first surface. The adjacent section includes a portion of the dopant impurities, and a distribution of the portion of dopant impurities within the adjacent section is uniform. The active area includes a source/drain region of a **transistor** .

INORGANIC CHEMISTRY - Preferred Material: The high- **diffusion**

grain structure comprises polycrystalline silicon adjacent region. The first surface is roughened by treating with dilute hydrofluoric acid.

Title Terms: SEMICONDUCTOR; DEVICE; DYNAMIC; RANDOM; ACCESS; MEMORY; DEVICE ; FORMING; SEMICONDUCTOR; SUBSTRATE; COMPRISE; **TRENCH** ; CAPACITOR; ACTIVE; AREA; FIRST; SURFACE; ROUGH; PRIOR; BURY; **STRAP** ; FORMATION; BURY; **STRAP**

Derwent Class: L03; U11; U12; U13; U14

International Patent Class (Main): H01L-027/108

International Patent Class (Additional): H01L-023/48

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C07E; L04-C14A

Manual Codes (EPI/S-X): U11-C18B5; U12-C02A1; U12-C02X; U12-Q; U13-C04B1A; U14-A03B4

?t s13/9/5

13/9/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009527137 **Image available**
WPI Acc No: 1993-220677/199328
XRPX Acc No: N93-169109
Substrate plate trench **capacitor** DRAM **cell array - has buried plate electrode in electrically and physically isolated region of substrate so that access** transistors **operate independently from other devices**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: KENNEY D M
Number of Countries: 009 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 550870	A1	19930714	EP 92121739	A	19921221	199328	B
JP 5283640	A	19931029	JP 92347663	A	19921228	199348	
US 5264716	A	19931123	US 92819148	A	19920109	199348	
TW 222716	A	19940421	TW 93100128	A	19930111	199422	
CN 1076310	A	19930915	CN 93100210	A	19930107	199424	
US 5348905	A	19940920	US 92819148	A	19920109	199437	
			US 93112406	A	19930826		
SG 44361	A1	19971219	SG 952309	A	19921221	199808	
KR 9704951	B1	19970410	KR 93133	A	19930107	199938	
CN 1262526	A	20000809	CN 99123542	A	19991111	200055	

Priority Applications (No Type Date): US 92819148 A 19920109; US 93112406 A 19930826
Cited Patents: 01Jnl.Ref; JP 1119057
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 550870	A1	E	15	H01L-027/108	
Designated States (Regional): DE FR GB					
JP 5283640	A			H01L-027/108	
US 5264716	A		12	H01L-027/108	
TW 222716	A			H01L-031/042	
CN 1076310	A			H01L-027/108	
US 5348905	A		14	H01L-021/70	Div ex application US 92819148 Div ex patent US 5264716
SG 44361	A1			H01L-027/108	
KR 9704951	B1			H01L-027/108	
CN 1262526	A			H01L-027/108	

Abstract (Basic): EP 550870 A

The memory cell includes an n-channel transfer device (14) formed in a p-type well (12) on the upper surface of a p-type semiconductor substrate (10). A control gate (16) couples data between a data or bit line diffused n-type region (18) and a diffused n-type storage node region (20) through the well.

In fabrication, a storage capacitor is formed in a deep **trench** (22) adjacent to the access **transistor** storage node (20) and includes a signal storage node formed by a conductive n-type polysilicon electrode (24) connected to the surface node (20) by a conductive **strap** (26). A thick insulating collar (28) increases the threshold voltage of the vertical parasitic FET formed within the p-well. Local surface isolation (30) defines active device regions.

ADVANTAGE - Reduces complexity of design, allowing process simplicity and increased yield; high density for e.g. 16Mbit and larger.

Dwg.1/12

Abstract (Equivalent): US 5264716 A

The high density substrate plate **DRAM** cell has a buried plate region formed in an electrically and physically isolated region of the semiconductor substrate, adjacent to deep **trench** capacitors so that the substrate region of **DRAM** transfer FETs is electrically isolated

from other FETs on a semiconductor substrate.

The buried region is partially formed by lateral out- **diffusion** from the **sidewalls** of the deep **trenches** and partially formed by an N-well surface **diffusion** which entirely surrounds the **DRAM** array region.

ADVANTAGE - Minimise charge leakage, optimised device bias.

Dwg.1/12

US 5348905 A

The method comprises of providing a semiconductor substrate of a first conductivity type, and forming a plurality of deep **trenches** in a matrix pattern on a top surface of the substrate. Then diffusing a second conductivity type impurity from the lower portion of the depth of the deep **trenches** into the substrate to form a continuous buried diffused region of a second conductivity type across the entire extent of the matrix pattern. Then forming a dielectric layer on the inside of the deep **trenches** and filling the **trenches** with a conductive electrode material.

Then forming around the perimeter of the matrix pattern a diffused surface region of the second conductivity type having a depth, so as to physically and electrically isolate a portion of the substrate in the matrix pattern above the continuous buried diffused region. Finally forming within the isolated portion of the matrix pattern of semiconductor devices for coupling signals to and from the conductive electrode material in at least some of the deep **trenches** .

ADVANTAGE - Provides a buried plate SPT **DRAM** cell array in which the density limitations of the prior art are removed. Allows process simplicity and thus increased product yield, which has a minimum impact on existing processing technologies.

Dwg.1/12

Title Terms: SUBSTRATE; PLATE; **TRENCH** ; CAPACITOR; **DRAM** ; CELL; ARRAY; BURY; PLATE; ELECTRODE; ELECTRIC; PHYSICAL; ISOLATE; REGION; SUBSTRATE; SO; ACCESS; **TRANSISTOR** ; OPERATE; INDEPENDENT; DEVICE

Derwent Class: U11; U13; U14

International Patent Class (Main): H01L-021/70; H01L-027/108; H01L-031/042

International Patent Class (Additional): H01G-004/06; H01L-021/82; H01L-027/04; H01L-029/00; H01L-029/76

File Segment: EPI

Manual Codes (EPI/S-X): U11-C18B5; U13-C04B1A; U13-D03A; U14-A03B4

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?t s13/9/2

13/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014140145 **Image available**
WPI Acc No: 2001-624356/200172
XRAM Acc No: C01-186159
XRPX Acc No: N01-465158
Dense memory cell, e.g. dynamic random access memory **cell, comprises dielectric-filled isolation** trenches **in striped pattern at** transistor
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DIVAKARUNI R; MANDELMAN J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6281539	B1	20010828	US 2000540854	A	20000331	200172	B

Priority Applications (No Type Date): US 2000540854 A 20000331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6281539	B1		24	H01L-027/108	

Abstract (Basic): US 6281539 B1

NOVELTY - A 6F2 memory cell comprises dielectric-filled isolation **trenches** in a striped pattern at transfer **transistors** and being spaced apart by uniform spacing.

DETAILED DESCRIPTION - A 6F2 memory cell comprises capacitors, each located in a separate **trench** that is formed in a semiconductor substrate. Transfer **transistors** are included, each having a vertical gate dielectric, a gate conductor, and a bitline **diffusion** . Each **transistor** is located above and electrically connected to a respective **trench** capacitor. Dielectric-filled isolation **trenches** are included in a striped pattern at the **transistors** , and are spaced apart by uniform spacing. A respective wordline is electrically contacted to each respective gate conductor, and is in the same direction as the isolation **trenches** . Bitlines are included which are in contact with the bitline **diffusions** . The bitline **diffusions** having a width that is defined by the spacing of the isolation **trenches** and active area of the transfer **transistors** are defined by the intersection of pairs of the isolation **trenches** and pairs of the **trenches** containing the capacitors.

USE - Used as a 6F2 memory cell, e.g. **dynamic random access memory** .

ADVANTAGE - The memory cell is scalable to a minimum feature size of 100 nm, and eliminates dynamic leakage due to adjacent cell activity. It has a large deep **trench** size for large storage capacitance, reduced resistance, and ease of fabrication. It contains an array **trench** isolation pattern that has reduced aspect ratio for simplified filling.

DESCRIPTION OF DRAWING(S) - The figure shows a preferred layout for the 6F2 memory cell.

pp; 24 DwgNo 16, 18/18

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The capacitor includes at least a plate electrode at an exterior region of the **trench** , a storage node dielectric layer lining the **trench** , and an interior electrode composed of N+ polysilicon. The capacitors and the transfer **transistors** are separated in the **trench** by a collar isolation region. A **diffusion strap** is located on one **sidewall** of the **trench** above the collar isolation region. The substrate further includes an N-band region at a lower region of the **trench** where the capacitor is located. A P-well is formed above the N-band region. A field doping region is formed beneath each isolation **trench** . The wordline comprises at least a wordline conductor, an oxide layer, and

spacers formed on **sidewalls** of the conductor and the oxide. The wordline are borderless to the underlying gate conductors.

INORGANIC CHEMISTRY - Preferred Materials: The substrate is composed of silicon (Si), germanium, silicon germanide (SiGe), gallium arsenide, indium arsenide, indium phosphide, Si/SiGe, or Si/silicon oxide/silicon, preferably Si. The bitline comprises tungsten or polysilicon

Title Terms: DENSE; MEMORY; CELL; DYNAMIC; RANDOM; ACCESS; MEMORY; CELL; COMPRISE; DIELECTRIC; FILLED; ISOLATE; **TRENCH** ; STRIPE; PATTERN; **TRANSISTOR**

Derwent Class: L03; U11; U12; U13; U14

International Patent Class (Main): H01L-027/108

International Patent Class (Additional): H01L-029/76; H01L-029/94; H01L-031/119

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C11C; L04-C12C; L04-C14A

Manual Codes (EPI/S-X): U11-C08A3; U12-A03; U12-C02A; U12-C02A1; U12-D02A; U12-Q; U13-C04B1A; U14-A03B4

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predetermined depth is 2000-5000 Angstrom beneath the surface of the substrate. The third predetermined depth is 3000-6000 Angstrom beneath the substrate surface. The fourth predetermined depth is 2000-5000 Angstrom beneath the substrate surface. The first insulating layer is composed of high density plasma (HDP) oxide having a thickness of 250-650 Angstrom. The second masking layer is a polysilicon layer having a thickness of 2500-4000 Angstrom. The second insulating layer is an oxide layer or HDP oxide layer having a thickness of 4000-7000 Angstrom. The third insulating layer is a thermal oxide layer formed by rapid thermal oxidation to a thickness of 50-150 Angstrom. The fourth insulating layer is a thermal oxide having a thickness of 50-150 Angstrom. The third conductive layer is doped polysilicon having a thickness of 650-1000 Angstrom. The fourth conductive layer has a thickness of 500-9020 Angstrom.

Title Terms: FABRICATE; DYNAMIC; RANDOM; ACCESS; MEMORY; CELL; **VERTICAL** ; TRANSISTOR; COMPRISE; CONTROL; DEPTH; **TRENCH** ; FORMING; GATE; **TRENCH** ; COVER; SURFACE; SUBSTRATE; SHALLOW; **TRENCH** ; ISOLATE

Derwent Class: L03; U11; U14

International Patent Class (Main): H01L-021/8238

International Patent Class (Additional): H01L-021/336; H01L-021/8242

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C11C1; L04-E01

Manual Codes (EPI/S-X): U11-C18A3; U11-C18B5; U14-A03B4

8/9/6 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014403711 **Image available**

WPI Acc No: 2002-224414/200228

XRAM Acc No: C02-068438

XRPX Acc No: N02-171879

Formation of buried straps **in deep trenches of set of memory cells in** dynamic random access memory **(DRAM) chip involves providing structure of silicon substrate, conformally depositing and dry etching collar layer**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: CORONEL P; LATTARD E; MACCAGNAN R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6297089	B1	20011002	US 99447630	A	19991123	200228	B

Priority Applications (No Type Date): EP 98480081 A 19981126

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6297089	B1		13	H01L-021/8242	

Abstract (Basic): US 6297089 B1

NOVELTY - Buried **straps** are formed in deep **trenches** of a set of memory cells by providing a structure consisting of a silicon substrate having a nitride pad layer with a set of deep **trenches** partially filled with a first layer of doped polysilicon, conformally depositing a tetraethyl orthosilicate-silicon dioxide collar layer above the doped polysilicon, and dry etching the collar layer.

DETAILED DESCRIPTION - Formation of buried **straps** in deep **trenches** of a set of memory cells in a **dynamic random access memory** (**DRAM**) chip comprises providing a structure (10) consisting of a silicon substrate (11) having a nitride pad layer with a set of deep **trenches** (14). The **trenches** are partially filled with a first layer of doped polysilicon having a dielectric film (15) interposed between the first layer of doped polysilicon fill (16) and the substrate to create the storage capacitor of the memory cell. A tetraethyl orthosilicate (TEOS)-silicon dioxide (SiO2) collar layer (18) is conformally deposited above the doped polysilicon, and dry etched to expose a top surface of the polysilicon fill and the

substrate in a buried **strap** (22') location at an upper portion of the **trench** . The collar layer is etched by:

(i) etching the TEOS with a high selectivity to TEOS at least 6 times faster than silicon nitride (12, 13), and stopping the etching process on the top surface of the pad layer; or

(ii) etching the TEOS partially isotropically to create a non negligible lateral etch component (V2) in addition to a **vertical** etch component (V1) and to expose a portion of the upper portion of the substrate on sidewalls of the **trench** , implanting a dopant in the upper portion of the substrate adjacent the **trench** to create a first element of the buried **strap** , filling the **trench** with a second layer of doped polysilicon so that the doped region and a doped polysilicon stud form the buried **strap** . The ratio between the **vertical** and the lateral etch components V1/V2 is 5-15.

USE - Forming buried **straps** in deep **trenches** of a set of memory cells in a **DRAM** chip.

ADVANTAGE - Eliminates POLY2/POLY3 interface, avoids formation of voids during POLY2 fill as dip-out phenomena disappears, and eliminates **vertical** leakage current and undercut in the SiO2 pad layer. It eliminates thermal oxide on buried **strap** doped region exposed surface, and has no TEOS and thermal oxide residue observed at the bottom of the **trench** . It also exhibits product reliability, throughput improvements, and process flow simplification.

DESCRIPTION OF DRAWING(S) - The figure shows the structure undergoing the steps of the buried **strap** fabrication process.

Structure (10)
Silicon substrate (11)
Silicon nitride (12, 13)
Trenches (14)
Dielectric film (15)
Doped polysilicon fill (16)
Tetraethyl orthosilicate-silicon dioxide collar layer (18)
Buried **strap** (22')
pp; 13 DwgNo 4C/4

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The ratio between the **vertical** and the lateral etch components is 7. The etching step (ii) is performed using a power twice as that of step (i), and using a pressure of 1.25 times the pressure of step (i). The process further comprises planarizing the structure by chemical-mechanical polishing to remove the second layer of doped polysilicon, and etching the doped polysilicon below the surface of the substrate to form the polysilicon stud.

Title Terms: FORMATION; BURY; **STRAP** ; DEEP; **TRENCH** ; SET; MEMORY; CELL; DYNAMIC; RANDOM; ACCESS; MEMORY; **DRAM** ; CHIP; STRUCTURE; SILICON; SUBSTRATE; DEPOSIT; DRY; ETCH; COLLAR; LAYER

Derwent Class: L03; U11
International Patent Class (Main): H01L-021/8242
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C12C
Manual Codes (EPI/S-X): U11-C18B5

8/9/7 (Item 7 from file: 350)

014350894
WPI Acc No: 2002-171597/200222
XRAM Acc No: C02-053039
XRPX Acc No: N02-130526

Clearing of isolation collar from deep trench **while leaving at other surfaces of deep** trench **, by depositing barrier material and silicon layer, implanting dopant ions, etching the unimplanted silicon, and removing isolation collar**

Patent Assignee: INFINEON TECHNOLOGIES NORTH AMERICA CORP (INFN); INT BUSINESS MACHINES CORP (IBMC)

013940254 **Image available**
WPI Acc No: 2001-424468/200145
XRAM Acc No: C01-128417
XRPX Acc No: N01-314823

Fabrication of trench **capacitor useful in ultra large-scale integration devices involves forming additional polysilicon layer to increase its total surface area**

Patent Assignee: MOSEL VITELIC INC (MOSE-N)
Inventor: WANG T T; WEI H

Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6251722	B1	20010626	US 2000546800	A	20000411	200145	B
TW 426947	A	20010321	TW 99121730	A	19991209	200151	

Priority Applications (No Type Date): TW 99121730 A 19991209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6251722	B1		12	H01L-021/8242	
TW 426947	A			H01L-021/76	

Abstract (Basic): US 6251722 B1

NOVELTY - A **trench** capacitor is fabricated by **vertically** forming an additional polysilicon layer on a bottom portion to increase the total surface area of the **trench** capacitor.

DETAILED DESCRIPTION - Fabrication of a **trench** capacitor (3) comprises (a) forming a **trench** (32) having a bottom portion (32a) and a sidewall (39) on a semiconductor substrate (31); (b) forming a diffusion layer (33) in the substrate adjacent to a lower portion of the **trench** including a bottom portion and a predetermined region in the sidewall of the **trench** ; (c) forming a first polysilicon layer (34) on the bottom portion of the **trench** in a manner that a portion of the first polysilicon layer does not contact with the sidewall; (d) forming a first dielectric layer (351) to overlap the first polysilicon layer and the diffusion layer; and forming an upper electrode layer (36) for covering the first dielectric layer completely.

USE - The method is used for forming **trench** capacitors useful in ultra large scale integration (ULSI) technology, e.g. **dynamic random access memories** (**DRAM**). It can also be used in merged isolation and node **trench** cell (MINT) and buried **strap** structure.

ADVANTAGE - The **trench** capacitor has high capacitance for ULSI technology below the submicrometer scale. The structure of the **trench** capacitor can save at least 25% of the chip area and efficiently reduce the manufacture cost. The generation of a parasitic n-type metal oxide semiconductor (NMOS) or leakage current.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **trench** capacitor.

Trench capacitor (3)
Semiconductor substrate (31)
Trench (32)
Bottom portion (32a)
Diffusion layer (33)
First polysilicon layer (34)
Upper electrode layer (36)
Sidewall (39)
First dielectric layer (351)
pp; 12 DwgNo 3/16

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The upper electrode is a polysilicon layer. Preferred Method: The diffusion layer is formed by depositing a silicate glass layer in the **trench** , defining and etching the silicate glass layer in a manner that the silicate glass layer overlapped the bottom portion and a predetermined portion of the sidewall, depositing a passivation layer for overlapping the silicate glass layer, and thermal annealing to out diffuse impurities of the silicate glass layer into the substrate. The first

polysilicon is formed by removing a portion of the passivation layer and silicate glass layer to expose the diffusion layer at the bottom portion of the **trench** , forming a conducting polysilicon layer, etching back the conducting polysilicon layer to form the first polysilicon layer, and completely removing the passivation layer and the silicate glass layer. The thermal annealing is conducted at 1000-1100degreesC. The upper electrode layer is formed by forming a second polysilicon layer in the **trench** , etching back the second polysilicon layer to a predetermined depth, etching back the first dielectric layer to a predetermined depth, forming a second dielectric layer having a thickness larger than that of the first dielectric layer to cover the sidewall, and forming a third polysilicon layer to cover the second dielectric layer and the second polysilicon layer. The method further includes etching back the third polysilicon layer, wet etching back the second dielectric layer, and forming a fourth polysilicon layer to cover the second dielectric layer and the third polysilicon layer. The first and second dielectric layers are formed by chemical vapor deposition (CVD). The step of etching the first dielectric layer is performed by wet etching.

INORGANIC CHEMISTRY - Preferred Materials: The impurities are arsenic and the passivation layer is a tetraethylorthosilicate (TEOS) oxide layer. The first dielectric layer and the second dielectric layer are formed from silicon dioxide, silicon nitride, silicon dioxide/silicon nitride, or silicon dioxide/silicon nitride/silicon dioxide layers

Title Terms: FABRICATE; **TRENCH** ; CAPACITOR; USEFUL; ULTRA; SCALE; INTEGRATE; DEVICE; FORMING; ADD; LAYER; INCREASE; TOTAL; SURFACE; AREA
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/76; H01L-021/8242
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C07E; L04-C10B; L04-C14A
Manual Codes (EPI/S-X): U11-C18B5

9/9/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010213581 **Image available**
WPI Acc No: 1995-114835/199515
XRAM Acc No: C95-052393
XRPX Acc No: N95-090663
DRAM **cell mfr. - comprises forming temporary protective layer on substrate, etching** trench vertically **to first depth, exposing upper** trench **sidewalls, etc.**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: HSU L L; OGURA S; SHEPARD J F
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5395786	A	19950307	US 94269852	A	19940630	199515	B
EP 690496	A2	19960103	EP 95480053	A	19950427	199606	
JP 8046158	A	19960216	JP 95163613	A	19950629	199617	
TW 286437	A	19960921	TW 95101636	A	19950222	199706	

Priority Applications (No Type Date): US 94269852 A 19940630
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5395786	A		7	H01L-021/70	
EP 690496	A2	E	8	H01L-021/8242	
JP 8046158	A		6	H01L-027/108	
TW 286437	A			H01L-027/108	

Abstract (Basic): US 5395786 A
The process forms a **DRAM** cell in a semiconductor substrate of a first polarity. The process comprises: (a) forming a temporary

protective layer on a substrate; (b) etching a **trench** **vertically** to a first depth, exposing the upper **trench** sidewalls and first **trench** bottom; (c) expanding the **trench** horizontally by isotropic etching of the upper **trench** sidewalls under the temporary protective layer to form **trench** collar sidewalls displaced from the upper **trench** sidewalls by a side wall offset distance; (d) forming a layer of collar dielectric with a thickness equal to the sidewall offset distance on the collar sidewalls and on the first **trench** bottom; (e) removing the collar dielectric from the first **trench** bottom; (f) etching the **trench** through the first **trench** bottom to a final **trench** depth with a final **trench** bottom and lower **trench** sidewalls; (g) doping the lower **trench** sidewalls with a sidewall dose of the second polarity; (h) forming a **trench** dielectric on the lower **trench** sidewalls; (i) forming an inner electrode within **trench** etching the inner electrode and the collar dielectric to a **strap** depth, exposing a **strap** contact surface on a portion of the collar sidewalls and an electrode contact surface on the top of the inner electrode; (j) forming a conductive **strap** between the **strap** contact surface and the inner electrode; and (k) forming an access transistor with a **strap** contact electrode abutting the **strap** contact surface.

ADVANTAGE - Simplified **trench** process reduces cost and increases process latitude.

(Dwg.10/13

Title Terms: **DRAM** ; CELL; MANUFACTURE; COMPRISE; FORMING; TEMPORARY; PROTECT; LAYER; SUBSTRATE; ETCH; **TRENCH** ; **VERTICAL** ; FIRST; DEPTH; EXPOSE; UPPER; **TRENCH** ; SIDEWALL

Index Terms/Additional Words: **DYNA** **MIC_RA** **NDOM_ACC** **ESS_ME** ; RANDOM; ACCESS; MEMORY

Derwent Class: L03; U11; U13; U14

International Patent Class (Main): H01L-021/70; H01L-021/8242; H01L-027/108

International Patent Class (Additional): H01L-021/3065

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C07E; L04-C14A

Manual Codes (EPI/S-X): U11-C18B5; U13-C04B1A; U13-D03A; U14-A03B4

9/9/18 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009527137 **Image available**

WPI Acc No: 1993-220677/199328

XRPX Acc No: N93-169109

Substrate plate trench **capacitor** DRAM **cell array - has buried plate electrode in electrically and physically isolated region of substrate so that access transistors operate independently from other devices**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: KENNEY D M

Number of Countries: 009 Number of Patents: 009

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 550870	A1	19930714	EP 92121739	A	19921221	199328	B
JP 5283640	A	19931029	JP 92347663	A	19921228	199348	
US 5264716	A	19931123	US 92819148	A	19920109	199348	
TW 222716	A	19940421	TW 93100128	A	19930111	199422	
CN 1076310	A	19930915	CN 93100210	A	19930107	199424	
US 5348905	A	19940920	US 92819148	A	19920109	199437	
			US 93112406	A	19930826		
SG 44361	A1	19971219	SG 952309	A	19921221	199808	
KR 9704951	B1	19970410	KR 93133	A	19930107	199938	
CN 1262526	A	20000809	CN 99123542	A	19991111	200055	

Priority Applications (No Type Date): US 92819148 A 19920109; US 93112406 A 19930826

Cited Patents: 01Jnl.Ref; JP 1119057

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

EP 550870	A1 E	15	H01L-027/108		
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JP 5283640	A		H01L-027/108		
US 5264716	A	12	H01L-027/108		
TW 222716	A		H01L-031/042		
CN 1076310	A		H01L-027/108		
US 5348905	A	14	H01L-021/70	Div ex application US 92819148	
				Div ex patent US 5264716	
SG 44361	A1		H01L-027/108		
KR 9704951	B1		H01L-027/108		
CN 1262526	A		H01L-027/108		

Abstract (Basic): EP 550870 A

The memory cell includes an n-channel transfer device (14) formed in a p-type well (12) on the upper surface of a p-type semiconductor substrate (10). A control gate (16) couples data between a data or bit line diffused n-type region (18) and a diffused n-type storage node region (20) through the well.

In fabrication, a storage capacitor is formed in a deep **trench** (22) adjacent to the access transistor storage node (20) and includes a signal storage node formed by a conductive n-type polysilicon electrode (24) connected to the surface node (20) by a conductive **strap** (26). A thick insulating collar (28) increases the threshold voltage of the **vertical** parasitic FET formed within the p-well. Local surface isolation (30) defines active device regions.

ADVANTAGE - Reduces complexity of design, allowing process simplicity and increased yield; high density for e.g. 16Mbit and larger.

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Abstract (Equivalent): US 5264716 A

The high density substrate plate **DRAM** cell has a buried plate region formed in an electrically and physically isolated region of the semiconductor substrate, adjacent to deep **trench** capacitors so that the substrate region of **DRAM** transfer FETs is electrically isolated from other FETs on a semiconductor substrate.

The buried region is partially formed by lateral out-diffusion from the sidewalls of the deep **trenches** and partially formed by an N-well surface diffusion which entirely surrounds the **DRAM** array region.

ADVANTAGE - Minimise charge leakage, optimised device bias.

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US 5348905 A

The method comprises of providing a semiconductor substrate of a first conductivity type, and forming a plurality of deep **trenches** in a matrix pattern on a top surface of the substrate. Then diffusing a second conductivity type impurity from the lower portion of the depth of the deep **trenches** into the substrate to form a continuous buried diffused region of a second conductivity type across the entire extent of the matrix pattern. Then forming a dielectric layer on the inside of the deep **trenches** and filling the **trenches** with a conductive electrode material.

Then forming around the perimeter of the matrix pattern a diffused surface region of the second conductivity type having a depth, so as to physically and electrically isolate a portion of the substrate in the matrix pattern above the continuous buried diffused region. Finally forming within the isolated portion of the matrix pattern of semiconductor devices for coupling signals to and from the conductive electrode material in at least some of the deep **trenches** .

ADVANTAGE - Provides a buried plate SPT **DRAM** cell array in which the density limitations of the prior art are removed. Allows process simplicity and thus increased product yield, which has a minimum impact on existing processing technologies.

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Title Terms: SUBSTRATE; PLATE; **TRENCH** ; CAPACITOR; **DRAM** ; CELL; ARRAY; BURY; PLATE; ELECTRODE; ELECTRIC; PHYSICAL; ISOLATE; REGION; SUBSTRATE; SO; ACCESS; TRANSISTOR; OPERATE; INDEPENDENT; DEVICE

Derwent Class: U11; U13; U14

International Patent Class (Main): H01L-021/70; H01L-027/108; H01L-031/042